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A Chips Act for Europe

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Introduction

On 8 February 2022, the European Commission proposed a comprehensive set of measures for strengthening the EU's semiconductor ecosystem, the **European Chips Act**.[1] In this package, the Commission has adopted a **Communication**, outlining the rationale and the overall strategy, a proposal for a **Regulation** for adoption by co-legislators, a proposal for **amendments** to a Council Regulation establishing the KDT Joint Undertaking, and a **Recommendation** to Member States promoting actions for monitoring and mitigating disruptions in the semiconductor supply chain.

To complement the proposed package, and as provided for in the Better Regulation rules for cases where an Impact Assessment could not be prepared due to the urgency of an initiative, this Staff Working Document (SWD) aims to explain why Europe needs to act now to address shortcomings in key chip design and manufacturing competences and facilities to ensure its resilience against supply chain disruptions. This SWD also provides additional information concerning the rationale behind the proposed measures in the 3 pillars which are the foundations of the proposal and explains further their implementation. This would not have been possible without providing a panoramic description of the characteristics of the semiconductor value chain, key market and technology trends and opportunities, given the complexity of the technological context and of the semiconductor ecosystem.

The SWD also intends to elucidate on the ongoing **crisis** and the pivotal role semiconductors have acquired in the global context. Semiconductors are indeed at the centre of **geopolitical** interests. Leading economies are keen to secure their supply in the most advanced chips with significant investments, as this increasingly conditions their capacity to act economically, industrially, militarily, being the drivers of the digital transformation.

The first part of the SWD (chapter 1) illustrates the highly complex semiconductor value chain, in which extraordinary technological advances have pushed to a high level of specialisation in a global network of deeply interdependent actors, with little flexibility leading to structural vulnerabilities and chokepoints. As consequence, the supply chain is prone to disruptions, such as the one that followed the pandemic and that is still ongoing, impacting many industries globally (as illustrated in chapter 2).

An analysis of the global semiconductors market, its main segments and future trends is outlined in Chapter 3, with a focus on the relative position of Europe. An overview of the main technology trends in key industrial sectors (chapter 4) is followed by an analysis of opportunities driven by the evolution of key technologies (chapter 5). Technological advances will be instrumental to help achieve Europe's 2030 ambitions (chapter 6), including the doubling of its production share of semiconductors, as set out in the Digital Decade targets[2], as well as the twin transition related to the electrification and digitalisation of the economy.

Against this backdrop and based on the conclusions (chapter 7) of the in-depth analysis, this SWD outlines a strategic approach, explaining the activities included in the Chips Act structured around three pillars. Chapter 8 provides further explanations on the set of measures included in these three pillars of the Chips Act:

[1] COM(2022) 45. Communication from the Commission: A Chips Act for Europe. 08/02/2022
COM(2022) 46. Proposal for a Regulation establishing a framework of measures for strengthening Europe's semiconductor ecosystem (Chips Act). 08/02/2022
COM(2022) 782. Commission Recommendation on a common Union toolbox to address semiconductor shortages and an EU mechanism for monitoring the semiconductor ecosystem. 08/02/2022
[2] COM(2021)118. 2030 Digital Compass: the European way for the Digital Decade. 09/03/2021

- **Pillar 1 -** The **Chips for Europe** Initiative supporting large-scale technological capacity building and innovation throughout the Union to enable the development and deployment of cutting-edge, next generation semiconductor and quantum technologies.
- **Pillar 2** aiming to create a framework to ensure **security of supply** by targeting the attraction of investments and enhanced production capacities in semiconductor manufacturing, advanced packaging, test, and assembly.
- **Pillar 3** proposing to create a coordination mechanism between the Member States and the Commission to strengthen collaboration with, and across, Member States for **Monitoring and Crisis Response**.

Governance and budgetary aspects are outlined in chapters 9 and 10. The SWD includes a glossary of terms and acronyms, and Annexes providing technical information in relevant aspects:

Annex 1. Introduction to Semiconductors providing some insight on the technology and different types of semiconductor devices.

Annex 2. Semiconductor Manufacturing describing the various steps of the fabrication process.

Annex 3. Moore's Law and its central role in the fast technology evolution of the sector.

Annex 4. FinFET and FDSOI Semiconductor Technologies. A comparative analysis of the two most prominent manufacturing technologies

Annex 5. Ongoing Pilot Lines with brief description of pilot lines launched in the period 2014-2020.

Annex 6. Chips for Europe: Examples of impact of Pilot Lines and their extended geographic and community benefits.

PART I

1. The Worldwide Semiconductor Manufacturing Landscape

1.1 Societal Dependence on Semiconductors

Semiconductors are the material basis for chips[3] embedded in virtually every technology product today. Chips are miniaturised physical devices that can capture, store, process and act on data. Semiconductors are essential building blocks for digital products used in everyday activities such as work, education and entertainment, for critical applications in cars, trains, aircraft, healthcare and automation, as well as for the functioning of key infrastructures for energy, mobility, data and communications. They are also crucial for the must-win technologies of the future, such as artificial intelligence (AI), low power computing, 5G/6G communications, as well as the Internet of Things (IoT) and edge, cloud and high-performance computing platforms.

A vast range of semiconductor devices are used in sensing, communications, power management and to meet ever-increasing computational demands as AI penetrates more and more application domains[4]. These miniaturised devices determine the performance characteristics of digital systems, not only in terms of computational throughput, but also in terms of security and energy-efficiency. With an increasingly connected world, security has become a key concern and essential in critical applications such as autonomous cars, electrical grid infrastructures and banking. The importance of ever-greater energy efficiency as an essential component of meeting the goals of the digital and green transitions has been highlighted in recent EU flagship initiatives[5,6].

All industrial ecosystems rely increasingly on semiconductor technology for their competitive edge. Top Original Equipment Manufacturers and social media companies have taken to designing their own chips in-house. The acquisition of suppliers, rivals and start-ups with semiconductor expertise has become part of a strategy for companies to enhance digital product offerings and accelerate next-generation production portfolios.

The massive investments in the world's major semiconductor-producing regions today are not just about the semiconductor industry per se, but about the enabling role of cutting-edge semiconductor technology in the competitiveness of downstream industries, in defending strategic economic interests and national security and delivering on societal challenges.

Ensuring security of supply and resilience across the full supply chain for these vital products is essential for Europe's future.

Semiconductors are at the heart of innovation and the current industrial revolution. A key enabler for the digitisation of industry and an essential element of future smart and sustainable products and services, they are critical to Europe's security and resilience of the semiconductor supply chain, and its economic and societal well-being.

[3] Also referred to as integrated circuits or ICs

[4] Communication from the Commission to the European Parliament, the Council, the European Economic and Social Committee and the Committee of the Regions 2030 Digital Compass: the European way for the Digital Decade, COM(2021) 118, 9.3.2021.

[5] Communication from the Commission to the European Parliament, the European Council, the Council, the European Economic and Social Committee and the Committee of the Regions. The European Green Deal. COM(2019) 640, 11.12.2019.

[6] A new Industrial Strategy for a globally competitive, green and digital Europe and its update of 2021 (https://ec.europa.eu/commission/presscorner/detail/en/IP_21_1884).

1.2 Global Semiconductor Value Chain

1.2.1 The major segments of the value chain

The active component of a chip is a transistor - an electronically controlled switch. Since the 1960s, the business of chip production has been driven by doubling the amount of transistors in a given area of semiconductor - and hence doubling the computing power without cost - every eighteen months. Referred to as Moore's Law (see Annex 3), this trend dates from 1965 when a chip had just 64 transistors.

The business is characterised by rapid technological change fuelled by constant research and development (R&D) at all stages of the value chain : from the **software** and intellectual property (**IP**)[7] that support the process of chip **design**, to the **materials** (wafers & chemicals) and **equipment** that support the processes of **fabrication**, and subsequent **assembly, test and packaging** of the chip.

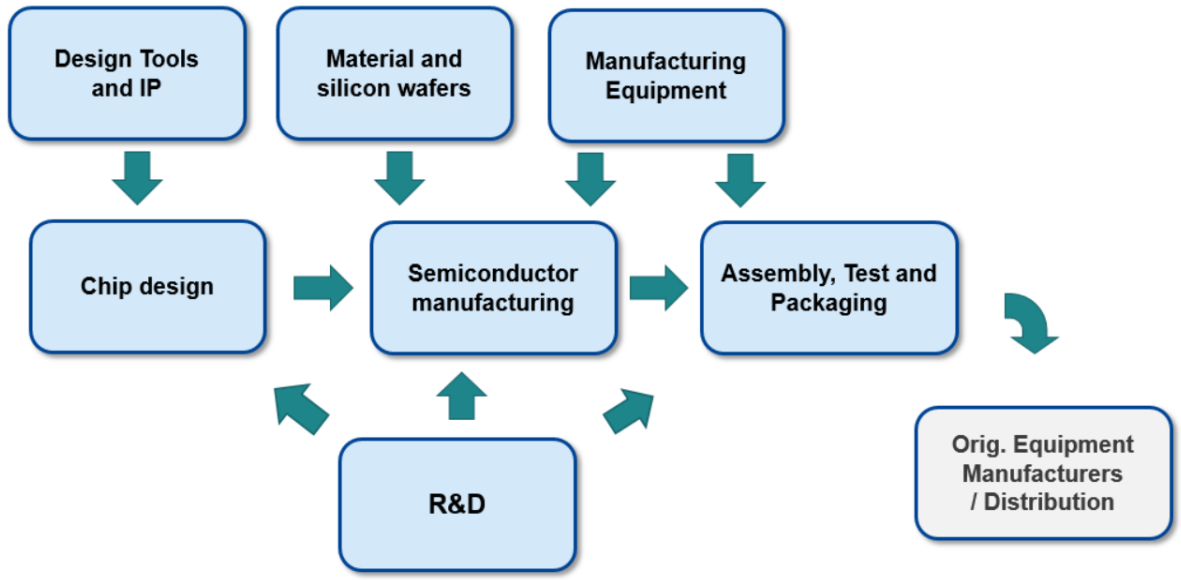

Figure 1. The semiconductor value chain

The process of chip **design** depends on specialised software tools or electronic design automation **(EDA) tools** provided by companies such as Cadence Design Systems, Synopsis and Mentor Graphics/Siemens. The EDA market is dominated by US companies with 70% of global sales. These tools use Intellectual Property blocks **(IP blocks)** from third-party IP vendors such as ARM (UK) or Imagination Technologies (UK) as parts of new designs.

Chemicals[8], specialty gases[9], minerals and high-purity materials are important for many of the process steps in semiconductor fabrication (e.g., patterning, deposition, etching, polishing) and for equipment operation, facility cleaning and packaging. Chip manufacturing requires nearly 500 specialised process

[7] Because of the complexity of designing chips with millions or even billions of transistors, chip designers license intellectual property or IP blocks (basic functional building blocks).
[8] Boron, Phosphorus, Germanium, Indium, Gallium, etc.
[9] Neon, Argon, Ammonia, Helium, Chlorine, etc.

chemicals; this number is rising as semiconductors become more complex. Key suppliers are Shin-Etsu Chemicals, Sumitomo Chemicals, Mitsui Chemicals (Japan), BASF, Linde, Merck KGaA, Air Liquide (EU), Taiwan Specialty Chemicals Corporation, and in Dow/DuPont (US). The demand for raw materials within the industry is expected to rise by more than a third in the next four years.

Silicon wafers serve as the substrate material and undergo a variety of complex process steps before being diced and packaged as chips. Depending of the production processes and input material used, there are different types of silicon wafers, with features and performance characteristics suitable for different end use chips. Japan's Shin-Etsu and Sumco are the world's largest silicon wafer makers respectively, followed by Taiwan's GlobalWafers, Germany's Siltronic, Korea's SK Siltron and France's Soitec.

Specialist vendors provide more than 50 different types of sophisticated **equipment** for each step in the chip fabrication process. Among them are lithography tools which determine the process node[10] size at which a semiconductor fabrication plant (fab) can produce, metrology and inspection equipment to confirm the yield over various stages of the process, different advanced automation and process control systems used for direct equipment control, automated transportation of materials and real-time dispatching of lots. Key suppliers include ASML (NL), Applied Materials (US), Tokyo Electron (JP), Lam Research (US), KLA Tencor (US) ASM-I (NL). The supply of certain pieces of equipment is extremely concentrated: for example, ASML holds a worldwide market share above 80% in the supply of lithography equipment, with a peak of 100% in the Extreme ultra-violet (EUV) lithography equipment.[11]

Annex 1 provides an introduction to the semiconductor technology and the different types of semiconductor devices.

Fabrication facilities, or front-end manufacturing[12], equipped with the most modern process technologies can enable transistors to be patterned onto the wafer to a precision of 5 nanometres (nm) or below and chips to be produced with 10s of billions transistors. The cost of building such a fab can be up to EUR 20 billion, while designing and developing such complex chips can be in the range of EUR 1 billion.

The volume required for cost-effective manufacturing is so high that many companies outsource production of their design to contract manufacturing companies that specialise in operating foundries for third parties. TSMC (TW), Samsung (KR), UMC (TW), SMIC (CN) and Global Foundries (US) are the major foundry companies[13]; however only TSMC and Samsung are currently able to offer front-end manufacturing at 5 nm and below.

[10] In semiconductor manufacturing, the process technology (or process node) has traditionally been correlated with the transistor dimension. It is measured in nanometres: 1nm or 1 nanometre = 1 billionth of a meter. **Smaller process nodes produce smaller transistors, which are faster in terms of computational throughput and more power efficient**. The smallest node in production today is 5 nm. The numbers are not related to physical features any more, but express the level of density of transistors for marketing purposes.

[11] Moody's, December 2020 (https://www.asml.com/-/media/asml/files/investors/shareholders/bonds-credit-rating/2020-12-17_asml_co_moodys.pdf)

[12] The fabrication of semiconductors is usually divided in two main phases. Front-end manufacturing refers to the wafer fabrication which includes processes such as photo-masking, etching, diffusion, ionic implantation, metal deposition, passivation (all of which are repeated many times), then backlap, and wafer probing. In back-end manufacturing, the wafer is cut, assembled, packed into different packages and tested; it is often called Assembly, Testing and Packaging (ATP).

[13] A semiconductor foundry is a producer of chips designed by others.

This has transformed the business dramatically. Previously such business was predominantly featured by Integrated Device Manufacturers (IDMs) who design their own chips and have their own facilities for fabrication and assembly. Today many companies run their businesses based on "fabless" or "fab-lite" models whereby they outsource all or some of their fabrication to foundries. Fabless design accounts for around 40% of global chip revenues with Qualcomm, Nvidia, Broadcom (US), MediaTek (TW) and AMD (US) as market leaders.

IDMs such as Intel (US), Micron (US), NXP (NL), Texas Instruments (US), STMicroelectronics (FR/IT) and Infineon (DE) perform front-end manufacturing in-house. These companies operate semiconductor wafer fabrication facilities, with typical volumes of 50,000-100,000 wafers per month[14]. Strictly speaking, IDMs also make use of third-party foundries, in particular for more advanced chips.

Annex 2 describes in detail the semiconductor fabrication process.

Back-end manufacturing includes the packaging of chips into a form that ensures reliability and enables connectivity with other circuit components. Each individual chip in the wafer is tested before the wafer is sliced into individual dies. The dies that pass the wafer test are packaged, and the packaged chips undergo a full functional and performance test. This is done in-house by semiconductor IDMs or via OSATs (Outsourced Semiconductor Assembly and Test)[15].

Figure 2 illustrates how revenues are distributed across the various segments across the value chain together with the levels of R&D and CAPEX spending as a percentage of revenues. Noteworthy is that chip design is the most R&D intensive segment accounting for 65% of total industry R&D, and fabrication (or front-end manufacturing) is the most CAPEX intensive segment accounting for 64% of total industry capex[16]. The value added also varies widely across the value chain (see chapter 3).

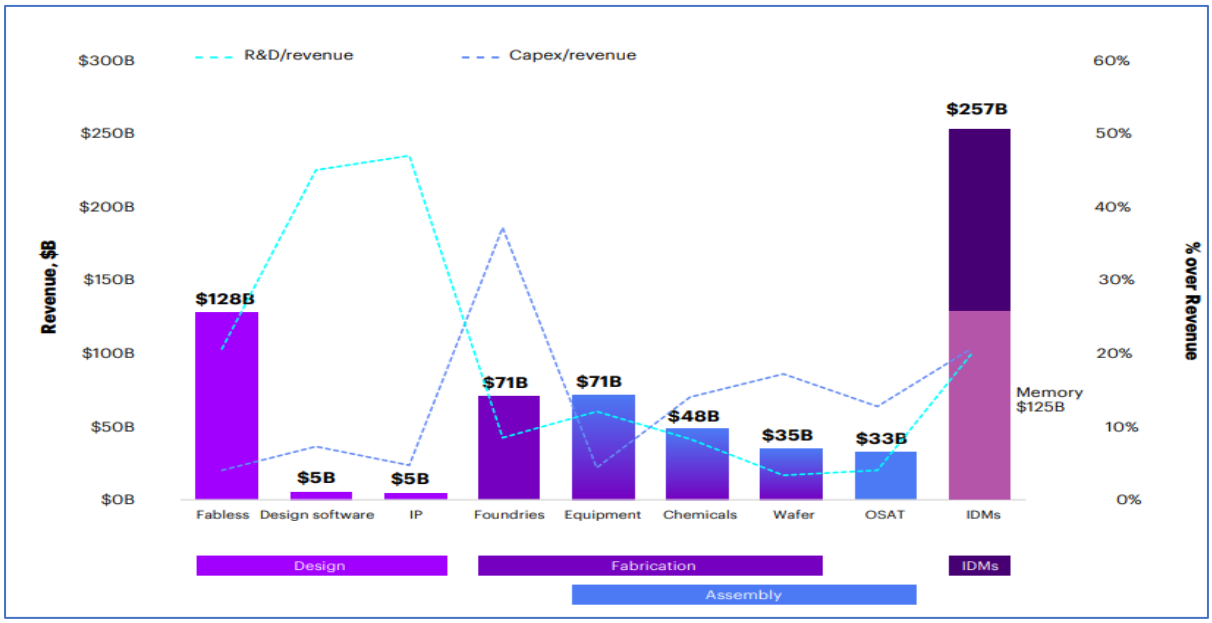

Figure 2. Revenue by Segment (Source: Accenture. 2022)

1.2.2 Interdependencies across the value chain

[14] At least 50,000 wafers per month for most modern fabs. Wafers are generally 300mm in diameter. One such wafer would hold 150 (giant) chips of 20x20mm. This would equate to 7.5 million chips per month.
[15] OSATs are companies that offer third-party IC packaging and test services. Major OSAT companies include ASE (Taiwan), Amkor (US) and JCET (China).
[16] BCG x SIA, "Strengthening the global semiconductor supply chain in an uncertain era", April 2021

It can be observed that at the current stage of the industry no single geography or company dominates all steps of the value chain. There will always be some parts of a system that require innovative solutions from another geographical region and this is unlikely to change, given the high level of capital expenditure required to ensure a given region could satisfy internal demand with only domestic supply across all levels of the value chain[17]. Thus, chip production relies on collaboration and trade between the major semiconductor-producing regions. It is a highly innovative and efficient value chain but, as shown in the following Chapter, is not resilient. Figure 3 illustrates the main steps in the production of chips with a large geographical dispersion and a myriad of interactions that are typical within the industry.

Figure 3 shows the example where a smartphone is produced for a customer in Argentina. IP blocks from the UK are designed into the chip using EDA tools in the US. The chip design is verified in India before being passed back to an Original Equipment Manufacturer (OEM) in the US who uses it in the smartphone design. The front-end manufacturing is carried out by a Taiwanese foundry using silicon wafers supplied from Japan, and European chemicals, specialty gases and equipment to produce a bare die. The die is then sent to Malaysia for back-end processing where it is packaged and then tested using equipment supplied by the US. The chip is assembled into the smartphone in China from where it is distributed through commercial channels to reach the final user in Argentina.

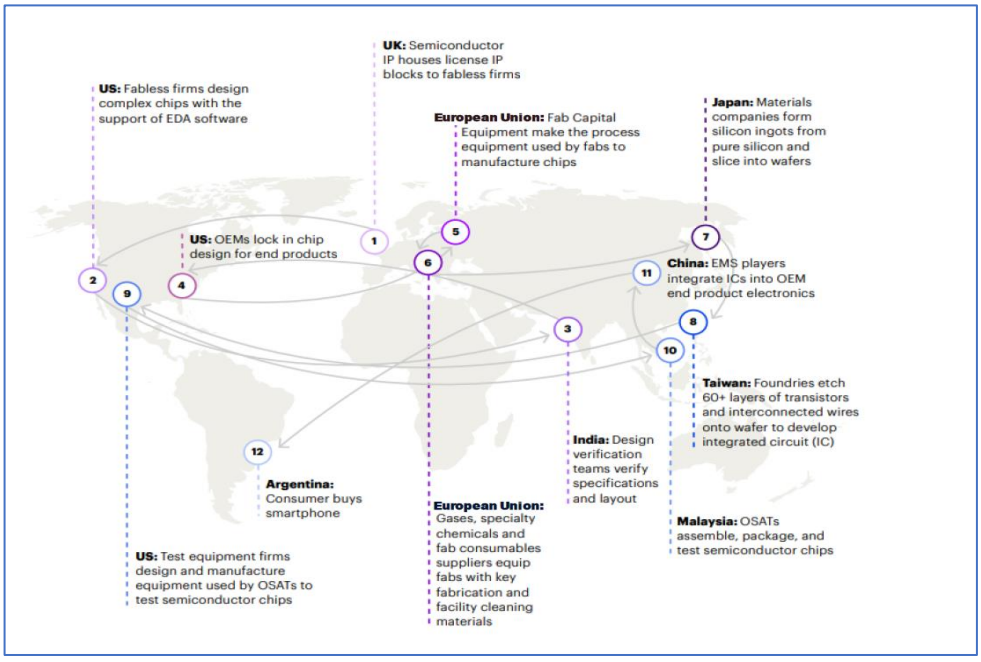

Figure 3. Illustrative example: Global Semiconductor Supply Chain for Smartphone (Source: Accenture. 2022)

Figure 4 is another example of the whole range of companies involved and the complex interdependencies for the production of chips for wireless and video processing applications.

[17] See BCG x SIA, "Strengthening the global semiconductor supply chain in an uncertain era", April 2021, Exhibit 21, estimating the cost of hypothetical semiconductor self-sufficiency by geographic area.

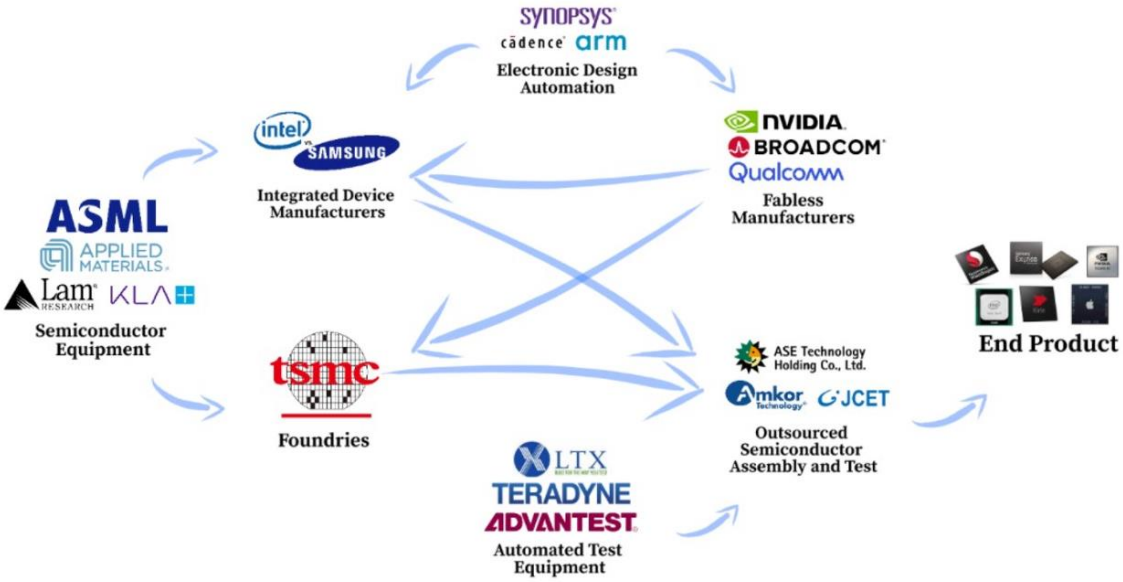

Figure 4. Complex interactions to develop wireless and video processing chips

1.2.3 Concentration and potential choke points within the supply chain

Producing a single chip requires up to 1500 process steps[18], each based on hundreds of variables. Some process steps during wafer fabrication, such as oxidation and coating, lithography, etching and doping, are repeated hundreds of times, depending on the specific chip. There are thus many points in the production process that are prone to disruption. Disruptions in semiconductor materials can have far-reaching ramifications across the value chain. For instance, in February 2019, a faulty batch of photoresist chemicals forced TSMC to scrap a large quantity of silicon wafers with a value of USD 550 million[19]. More recently, the closure of the 3M plant in Belgium, which produces fluorinated coolant for semiconductor manufacturing, has led to major concerns in the industry as there is no alternative supplier[20]. The most recent Chinese lockdown has had the effect that some raw materials and products are not being loaded and freighted from Shanghai, causing delays in various production sites worldwide.

Additionally, several levels of the supply chain are extremely concentrated, featuring limited alternatives for customers, which leads to strong lock-in effects. This creates the risk of single points of failure in supply chains with companies unable to find second or third source suppliers. For instance, TSMC in Taiwan and Samsung in South Korea are the only foundries capable of manufacturing the most advanced chips (at nodes below 5 nm) and ASML (NL) is the only supplier of advanced Extreme ultra-violet (EUV) lithography equipment. Currently there are more than 50 points in the global semiconductor value chain representing potential single points of failure. These represent more than 65% of the global market value[21].

East Asia is the most important region for back-end manufacturing (assembly, test and packaging) and this **high geographic concentration of companies increases the risk of supply chain disruptions**.

[18] Jan-Peter Kleinhans and Julia Hess, "Understanding the Global Chip Shortage", November 2021.
[19] In the electronics industry, materials take center stage (acs.org). Chemical and Engineering News.
[20] https://www.eetimes.com/3m-cuts-output-of-hazardous-material-used-in-chip-production/
[21] Semiconductor Industry Association. Input to the Department of Commerce on 'Semiconductor Manufacturing and Advanced Packaging Supply Chain'. 5th April 2021

For instance, Ajinomoto Build-up Film (ABF) substrates produced in Japan and Taiwan are essential for every chip that uses laminated packaging. ABF substrates connect different components within a chip and are widely used in chips for graphics cards, servers, smartphones, laptops, etc. Shortages have persisted for some time[22] and are causing delays in chip production as well as price increases.

Typically, front-end manufacturing of dies takes between 8 and 28 weeks, with the back-end processes of assembly and packaging taking 4 to 10 weeks, and testing taking another 2 weeks. In total, producing a semiconductor can take more than 6 months. Consequently, **the industry is characterised by long-term planning, with customers placing their orders well in advance, with very little flexibility for deviations.**

The semiconductor value chain is complex and global with many interdependencies, and relies on collaboration and trade between regions. The supply chain is however far from being resilient; disruptions at any point can have ramifications across the full value chain. Choke points may emanate from concentrations of specific essential technology within a single company or within a single geographical region.

[22] 41 Phil Garrou. 2021. "IFTLE 479: ABF Substrate Shortages; Consolidation Continues","IFTLE 479: ABF Substrate Shortages; Consolidation Continues", 3DInCites.

2. The Chips Crisis

2.1 Unprecedented Global Semiconductor Shortages

As highlighted in the previous chapter, semiconductor supply chains are highly interconnected with many actors across the globe and numerous choke points which can impact production. Over the past 2 years, Europe and other regions of the world have witnessed disruptions in the supply of chips, causing shortages across multiple economic sectors with potentially serious societal and economic consequences.

In a nutshell, the disruptions resulted from multiple factors, including the acceleration of digital transformation in industry leading to an increased demand in a large number of semiconductor components and devices; heightened demand for computers, electronics and technology products as lockdowns related to the COVID-19 pandemic led to a surge in remote working, home schooling and digital entertainment; COVID-19-related closures of key fabs; dislocations in global logistics and transportation networks coupled with shortages of raw materials, key components and intermediary products.

The shortage of chips has impacted downstream sectors such as automotive, energy, communications and health, as well as defence, security and space, forcing delays in production and factory closures across the world. The impact was severe and in the automotive sector, for instance, production in some European Member States decreased by one third in 2021[23].

2.2 Why has the supply chain become so fragile?

Since the turn of the century, the semiconductor industry has responded to market difficulties through consolidation and outsourcing to the Far East, particularly concerning production, and assembly and testing. **While this appears to have led to better utilisation of existing capacity, however it has reduced available spare capacity.** Thus, given the high capital expenditure and time required to set up new manufacturing facilities, there appears to be limited possibility to increase production if demand goes up considerably as it did from early 2020.

At the same time, the drive towards zero inventory approaches by some end user industries has led to a situation where in case of a sudden increase in demand for chips, there is very limited available inventory buffer to source from, until production can catch up. The result of this is a high susceptibility across the supply chain to surges in demand. A key problem is that once demand exceeds supply it takes at least 2-3 years to recover as there is a need for significant investment to increase capacity and inventory with a resulting long lead time for components.

In recent years, geopolitical tensions have been simmering. China depends on US-origin technology and imports of chips from Taiwan. With the "Made in China 2025" plan launched in 2015, China set itself the ambition of reaching 70% autonomy in chip-making by 2025 and to this end earmarked USD 150 billion to build up semiconductor design and manufacturing capacity. The creation of this fund has been linked to the growth in pace of cross-border acquisitions in the sector since 2015[24].

[23] William W. Pitkin, Jr. 2021. "Chip Shortages: Created by Demand, Geopolitics, Pandemic and Mother Nature". State Street Global Advisors.
[24] Measuring distortions in international markets: The semiconductor value chain, OECD December 2019

The U.S. government has responded to this "concerted push by China to reshape the market in its favour"[25]. In 2019, the US Department of Commerce broadened the application of its Export Administration Rules (EAR) to curb the technological advance of certain Chinese companies by cutting them off from critical US-origin technology. Because of Europe's strong dependence on US-origin technology for chip design however, these measures have impacted European chipmakers trading with China.

The shortages over the past two years have exposed structural vulnerabilities in highly interdependent and global value chains already weakened by lean production strategies and geopolitical frictions pre-dating the pandemic. They have furthermore served to highlight Europe's dependency on supply from a limited number of companies and geographies.

2.3 Factors in the Current Chip Crisis

From the onset of the COVID-19 pandemic in early 2020, the entire semiconductor business has seen a strong growth in demand. **Shipments of chips increased by 40%** from around 73 billion in 1Q20 to approximately 102 billion in 3Q21 (see Figure 5).

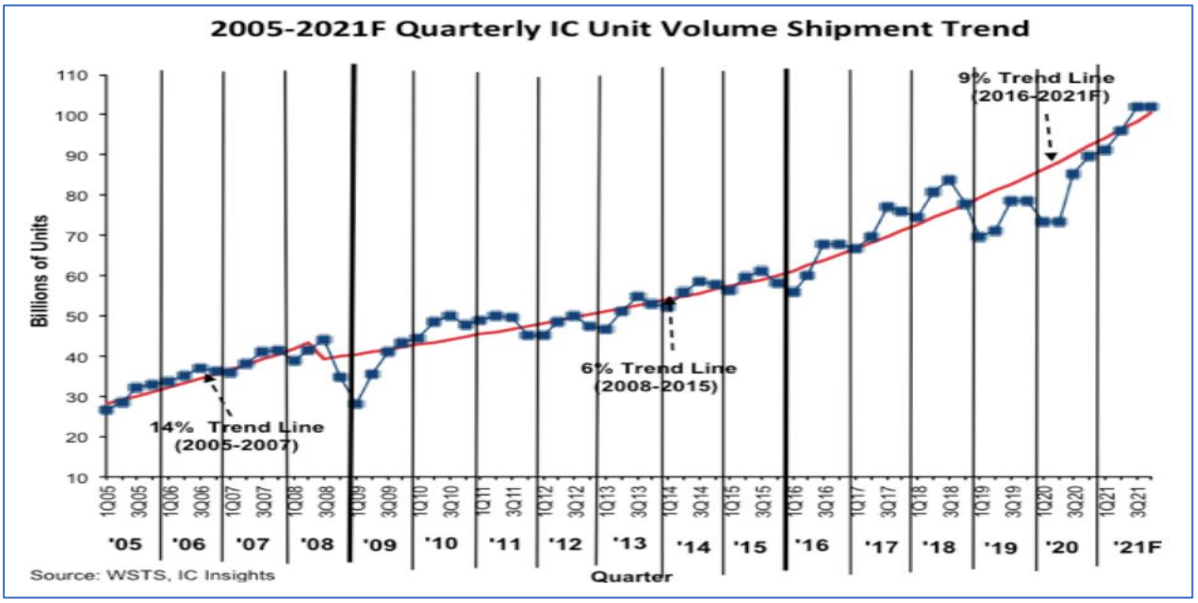

Figure 5. IC Unit Volume Shipment Trend (source WSTS, IC Insights)

With little spare capacity, it was not possible for the industry to react quickly to this surge in demand. It could be met partly by depleting the limited inventory that was available. As a result, across the world, **lead times for components doubled** from roughly 10 weeks to 20 weeks for microprocessors, memory chips, power management and analogue chips (see Figure 6).

[25] PCAST Ensuring Long-Term U.S. Leadership in Semiconductors, Report to the President. January 2017

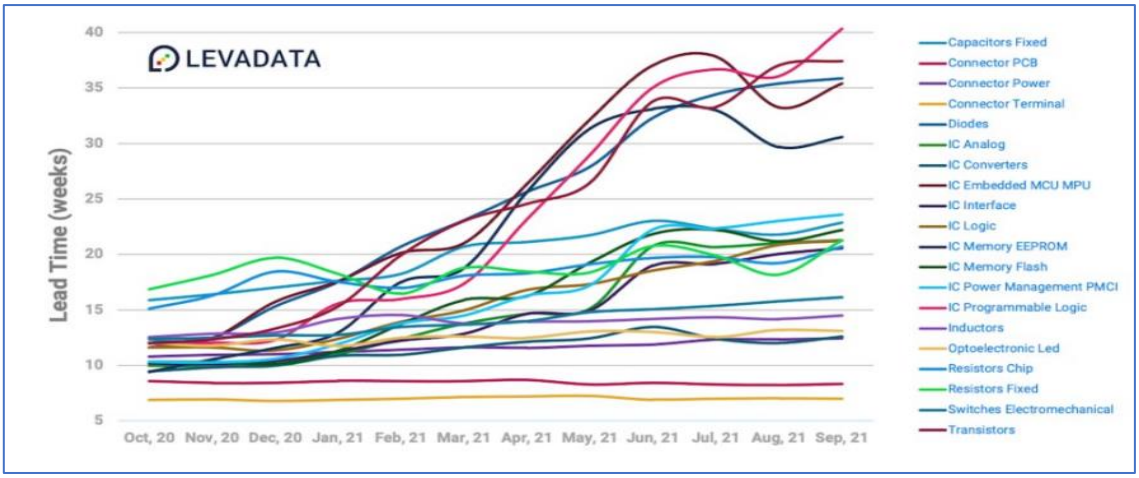

Figure 6. Increasing IC Lead Times During 2021

Demand has been further exacerbated by companies over-ordering and stockpiling components. To what extent stockpiling has moved future demand into the present is still unclear.

According to the Semiconductor Industry Association (SIA): "when market demand runs high, such as in a cyclical market upturn like the one the market is in now, front-end semiconductor fabrication facilities, or fabs, will typically run above 80 percent capacity utilization, with some individual fabs running as high as between 90-100 percent." As Figure 7 below shows, the industry has been steadily increasing overall fab utilization over the past two years and is estimated to have increased utilization even more during most of 2021 to meet demand.

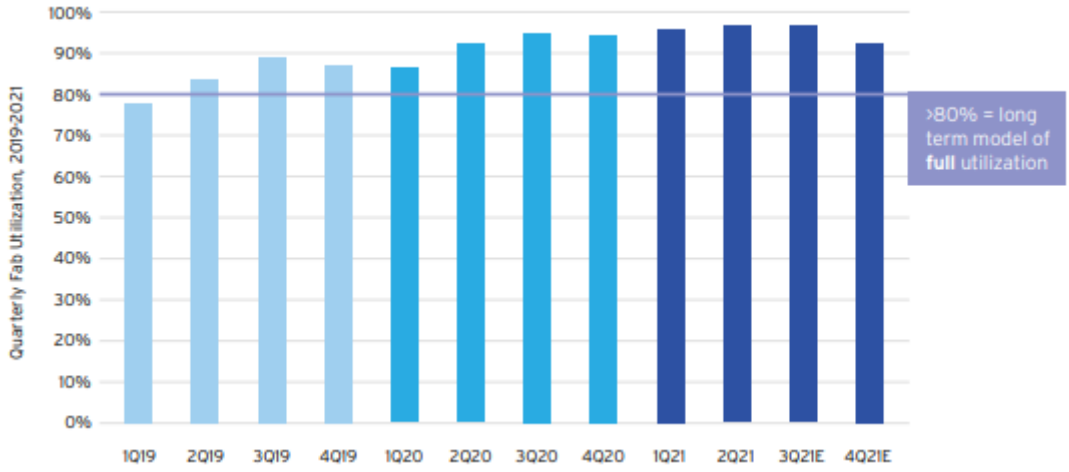

Figure 7. The industry has been steadily increasing overall fab utilization. (Source: SIA)

In addition to long term economic drivers that have reduced the flexibility of supply chains, there have also been a number of external shocks[26] and disruptions in the last two years including: earthquakes, the fire at the Renesas fab in Japan, ice storms in Texas, power outages at Infineon, NXP and Samsung fabs, as well as droughts in Taiwan and human errors.

[26] Fusion Worldwide. 2021. "The Global Chip Shortage: A Timeline of Unfortunate Events".

2.4 Impact of shortages

The impact of these shortages of components has been dramatic with implications in a number of critical areas such as supply of medical devices, devices for broadband communications and components for the automotive sector, just to mention a few. This includes shortages of microcontrollers (40, 90, 150, 180, and 250 nm nodes), analogue chips (40, 130, 160, 180, and 800 nm nodes) and optoelectronic chips (65, 110, and 180 nm nodes).

Figure 8 shows some of the markets affected by these different semiconductor shortages. Goldman Sachs estimates that around 169 industry sectors globally have been impacted[27]. **Within Europe, the automotive sector is a significant market (accounting for 37% of the semiconductor demand) as well as industrial manufacturing (accounting for 25% of semiconductor demand)**.

Figure 8. Markets for different Semiconductors (Source ZVEI-PK)

Other important European semiconductor end-use sectors include communications (15%) and consumer electronics (7%)[28]. **The shortages have led to European companies struggling to source**

[27] William W. Pitkin, Jr. 2021. "Chip Shortages: Created by Demand, Geopolitics, Pandemic and Mother Nature". State Street Global Advisors.
[28] Source: ZVEI-PK (see also section 3.2)

chips for cars[29] **and medical devices such as ultrasound equipment, pacemakers, ventilators, etc**[30]**.** The production of medical equipment has suffered chip supply disruptions resulting in a volume decrease for some medical systems of more than 70%[31].

A survey conducted by the European Commission[32] has shown that the vast majority of responding businesses reported being either directly or indirectly adversely affected by the current shortage in chips.

2.4.1 Example: the chips shortage and its impact on the automotive industry

Following COVID-19 lockdown measures and pessimistic demand forecasts for cars, automakers and their tier 1 (direct) suppliers cancelled orders during 1Q20 and 2Q20. When the rebound in demand for cars kicked in late 2020, the surge in demand for IT equipment generated by the COVID-19 crisis had already led to the world's largest foundry, TSMC, running at full capacity.

Other factors, notably geopolitics, had further exacerbated the situation. Under the Wassenaar agreement, the US had blocked Dutch-based ASML from shipping its EUV lithography equipment to China's major foundry, SMIC, preventing SMIC from advancing and growing to full capacity. At the same time, US chipmakers have had to shift their orders from SMIC to TSMC. Also faced with US sanctions, some Chinese chipmakers have been stockpiling in order to meet future demand.

As a volume business for TSMC, compared with automotive (which accounted for just 3% of its revenues in 2020), chips for IT equipment remained first in line.

The problems were then compounded by the limited resources in the value chain and the long manufacturing cycle times which are at odds with the "just in time" approach used in automotive. Additionally, automotive chips require stringent safety requirements (weather resistance, fault tolerance, redundancy, etc.) that must be certified, including the production process. This limited the number of fabs and packaging companies that automotive chip suppliers can utilise.

As a result, car companies are having to wait for periods of up to a year or more and car factories had to reduce production or shut down, laying off workers. In several EU Member States car production was severely affected: in the case of Germany, 2021 production fell by 34% when compared to 2019, back to 1975 levels[33]. In 2022, car production plans have been cut back and the lead times for chips are still twice as long as they were in 2019.

The above highlights the extreme dependency of Europe on the semiconductor value chain and the importance of a stable semiconductor supply chain for European industry.

The timeline of events and impacts for the automotive industry is shown for TSMC in Figure 9. This shows the major disruptions in chip manufacturing as supply chains were out of synchronisation with the demand from the automotive manufacturers. Vehicle demand came back strongly after the initial

[29] Mark Fulthrope and Phil Amsrud. 2021. "Global light vehicle production impacts now expected well into 2022". IHS Markit.
[30] Denise Roland. 2021. "Pacemaker, Ultrasound Companies Seek Priority Amid Chip Shortage". The Wallstreet Journal.
[31] Philips Healthcare
[32] In early 2022, the European Commission has carried out a targeted stakeholder survey ('EU Chips Survey') (https://ec.europa.eu/growth/news/stakeholder-survey-european-chip-demand-2022-02-16_en). The European Commission will publish an overview of the aggregated results of the EU Chips Survey as part of a Factual Summary Report during Q3 of 2022. These will help to provide crucial information on sources and impacts of the supply survey.
[33] Source: Verband der Automobilindustrie

disruptions in 1Q20 and 2Q20. Due to chips not being supplied in time, estimated drops in global output amounted to 1.4 million light vehicles 1Q21 and 2.6 million in 2Q21.

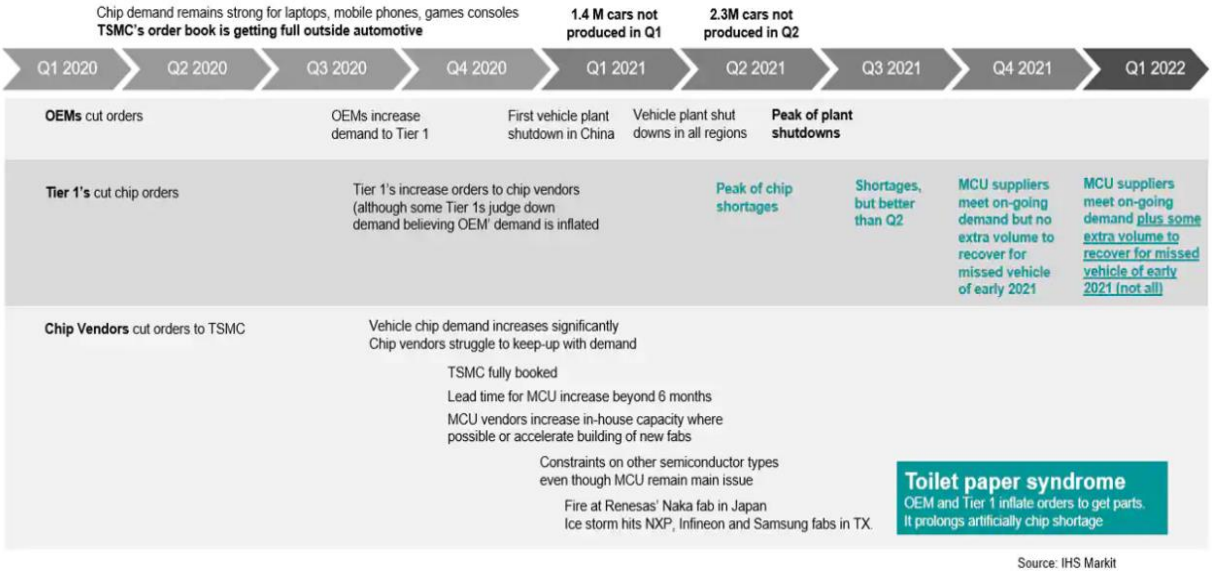

Figure 9. Impact on TSMC of variety of disturbances during 2020 and 2021(source IHS Markit)

In 2021 disruption continued and was aggravated by the effects of the ice storms that hit NXP in Texas, along with the fire at the Renesas Naka 3 facility in Japan (the fire in the 300 mm cleanroom impacted a small area of the fabrication, but it damaged water supply, air conditioning, and manufacturing equipment). Water is used heavily in chip manufacturing for cooling; the drought in Taiwan which led to water restrictions also affected production.

2.4.2 Example: the chips shortage and its impact on the healthcare industry

The COVID-19 pandemic has put Europe's healthcare system under severe strain. For providers of medical systems, shortages of chips have been of particular concern as they are used in medical devices and systems for patient monitoring, x-rays, ultrasound, computed tomography, image guided therapy, respiratory devices, emergency defibrillators and contrast media injectors.

Shortages of processors, converters, programmable and logic devices for the healthcare sector have been reported by COCIR[34]. Salient examples of chip shortages on healthcare are the lack of programmable components used to process and transfer images for patient diagnosis and treatment in Magnetic Resonance Imaging (MRI)[35], and the gap between the demand and supply for a specific microcontroller in Patient Monitoring Line (PML) systems[36] that prevents the installation of tens of thousands of beds in intensive care. Such components are all the more difficult to substitute when they are designed to be compliant with EU regulations such as the RoHS directive. In addition to short-term measures to alleviate the situation in Europe, it is essential to ensure the mid to long-term resilience of

[34] COCIR is the European Trade Association representing the medical imaging, radiotherapy, health ICT and electromedical industries. http://www.cocir.org/
[35] Siemens Healthcare. https://www.siemens-healthineers.com/
[36] Philips Healthcare. https://www.usa.philips.com/healthcare

the healthcare value chain, in which semiconductors is a critical input. This includes, for instance, priority access to key components in periods of crisis.

2.4.3 Example: The chip shortage and its impact on the EU space and defence

The space and defence domains are facing severe difficulties to procure components. As mentioned previously, semiconductor foundries give priority to markets with high volume demand, such as mobile handsets and IT equipment; space and defence account for approximately 1% of total market volume. The increased lead times during 2021 have had major effects on space missions and the deployment of services supported by EU space programmes (e.g. Galileo second generation, new sentinels part of Copernicus with advanced services for Earth environmental monitoring).

The strategic importance of these two sectors is significant for Europe, thus creating the urgency of reducing the dependence of the EU industry from non-EU semiconductor suppliers. The inability of EU space and defence industry to autonomous and unrestricted access to semiconductors could have a considerable impact on the competitiveness of the sector, the security of EU citizens and EU's strategic autonomy.

2.4.4 Example: The chip shortage and its impact on industrial automation

The European industry uses many different types of semiconductors for the machines and equipment it produces, and to support industrial automation and electrification the need for chips is steadily increasing. The machinery and equipment industry is one of the EU economy's most valuable assets and advanced technologies, such as machine vision and robotics, are essential to keeping it globally competitive. Electrification of the industry is also a key component of the green transition and of becoming less dependent on (imported) fossil fuels, as recently stated in the RePowerEU Communication[37] that is calling for decarbonising industry.

The European machinery and equipment industry has suffered considerably under supply shortages. Of the 5.1 percentage points shortfall in EU-wide industrial production in the first three quarters of 2021, the machinery and equipment sector bore 0.8 percentage points, just behind the automotive industry with 0.9 percentage points.[38]

There are hundreds of different types of machinery and equipment being produced in Europe. This large diversity of European manufacturers makes collective procurement, R&D and investment efforts more difficult. The needs and timelines of the manufacturers differ. Additionally, the industry is characterised by specialised companies, often SMEs, which have limited bargaining power.

Even key EU companies producing semiconductors manufacturing equipment, including ASML, have been affected, which in turn is hampering the needed expansion of global production capacity due to severe delays (up to 3 years) in the delivery of tools.

2.4.5 Example: The chip shortage and its impact on the EU energy system

The digitalisation of the energy network and its transformation towards green power is affected by the lack of some semiconductor components, such as programmable devices (FPGAs). The shortage impacts particularly small to mid-size technology suppliers that play an important role in the value

[37] https://eur-lex.europa.eu/legal-content/EN/TXT/?uri=COM%3A2022%3A108%3AFIN
[38] https://voxeu.org/article/impact-shortages-manufacturing-eu

chain,, as the limited demand of some of these critical users translates into low delivery priority for chip vendors. That also severely slows down the installation and operation of wind turbines and photovoltaic systems and their connection to renewable generators. Examples like this would affect the transformation of the European energy system, which is now even more urgently needed as a result of the Ukraine crisis.

2.5 Impact of the Ukraine Crisis

Russia's military aggression against Ukraine has had significant economic implications. Ukraine supplies various raw materials that are critical to chip manufacturing and that can be impacted by the current crisis: neon, palladium and C4F6[39].

Ukraine is a major source of inert gases, such as neon required for the semiconductor lithography process, and any disruption in the supply of neon and other noble gases could trigger shortages and associated cost inflation. Some 45%-54% of the world's semiconductor-grade neon, critical for the lasers used to make chips, comes from two Ukrainian companies, Ingas and Cryoin. They have halted their operations during to current crisis, which may lead to an increase of prices and aggravate the semiconductor shortage.

The stoppage impacts the worldwide output of chips, already in short supply after the coronavirus pandemic. While chipmakers keep some stocks of neon on hand, production could take a hit if the war continues.

Another effect has been the rise in price and likely disruption in the supply of natural gas, used as a source of power in fabs as well as for burning exhaust gases from the manufacturing process to make them safe. This will have a significant impact on operating costs.

The semiconductor industry uses air freight extensively. The flight bans over Russia have led to longer air freight routes, with corresponding cost increases and delays.

Russia is an important producer of metals like aluminium, nickel and copper. Aluminium is a conductor that is commonly used in packaging (wire bonding) and to manufacture passive components, such as resistors and capacitors, commonly used in all types of electronic equipment. Any disruption in the supply of any of these metals could cause prices to rise and subsequently impact the prices of semiconductor devices and electronic systems. However, it is important to note that most chip manufacturers have contingency plans, such as diversifying suppliers and maintaining high levels of inventory.

The global semiconductor value chain had already been weakened by lean production strategies and geopolitical frictions pre-dating the pandemic. The shortages have exposed structural vulnerabilities across highly interdependent supply chains and have furthermore served to highlight Europe's dependency on supply from a limited number of companies and geographies with severe consequences for many of its key industrial sectors.

[39] C4F6 Hexafluorobutadiene. A gas used in etch processing.

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PART 2/4

COMMISSION STAFF WORKING DOCUMENT

A Chips Act for Europe

3. Global Market Perspectives and where Europe is in the Market

3.1 Market Perspectives - World Markets

The semiconductor market in 2021 was worth **USD 555.9 billion**, according to World Semiconductor Trade Statistics (WSTS), with 1.15 trillion semiconductor components sold. This represents an increase of 26.2% with respect to 2020.

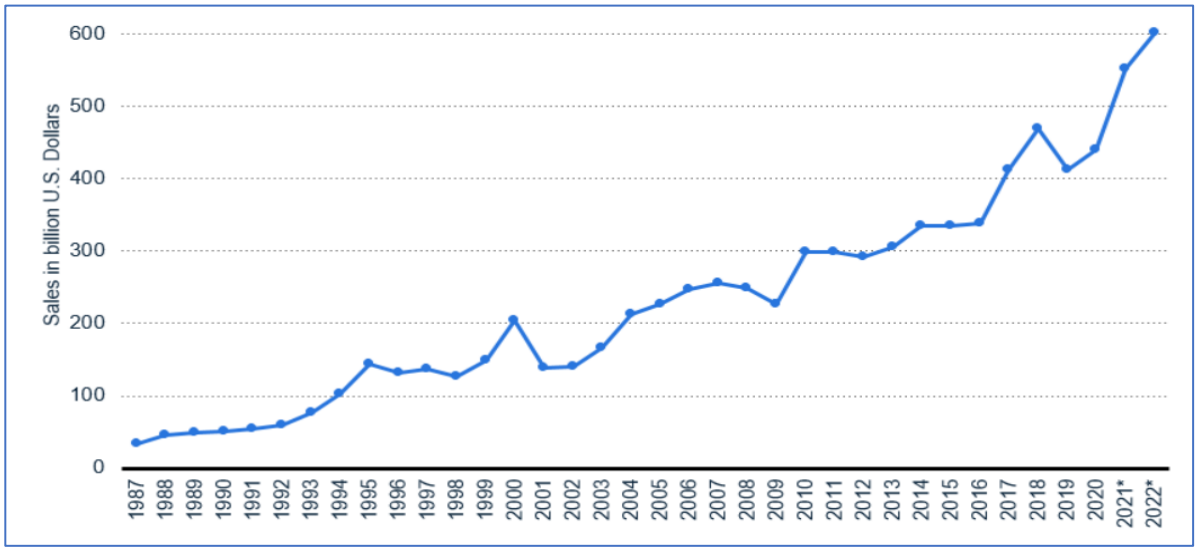

Figure 10. Semiconductor Industry Sales Worldwide 1987-2022 (Source: WSTS)

The market has been increasing rapidly as shown in Figure 10 and assuming that the CAGR of 7.1% of the last 20 years continues **until 2030, it is estimated that the market will exceed USD 1 trillion**. According to several sources[1], the total market value is expected to approximately double by 2030; some estimates go even beyond the above (see Figure 11).

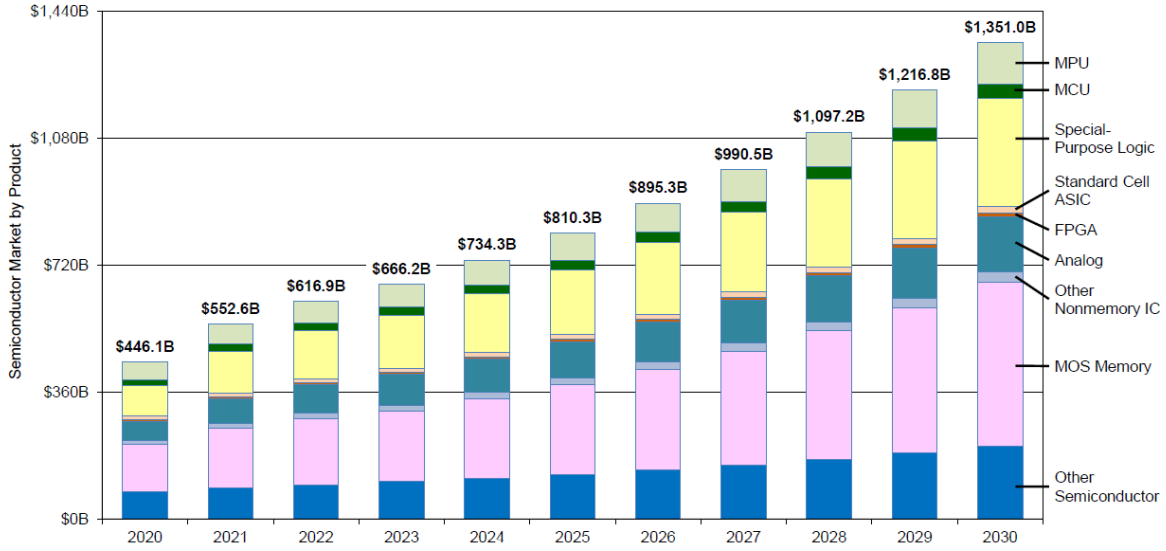

Figure 11. Semiconductors market forecast by product type (IBS 2022)

[1] SEMI, McKinsey, IBS, SIA and others.

The increasing demand expected in all regions is mostly due to the digital transformation and the constant growth of semiconductor content in electronic systems (see Figure 12).

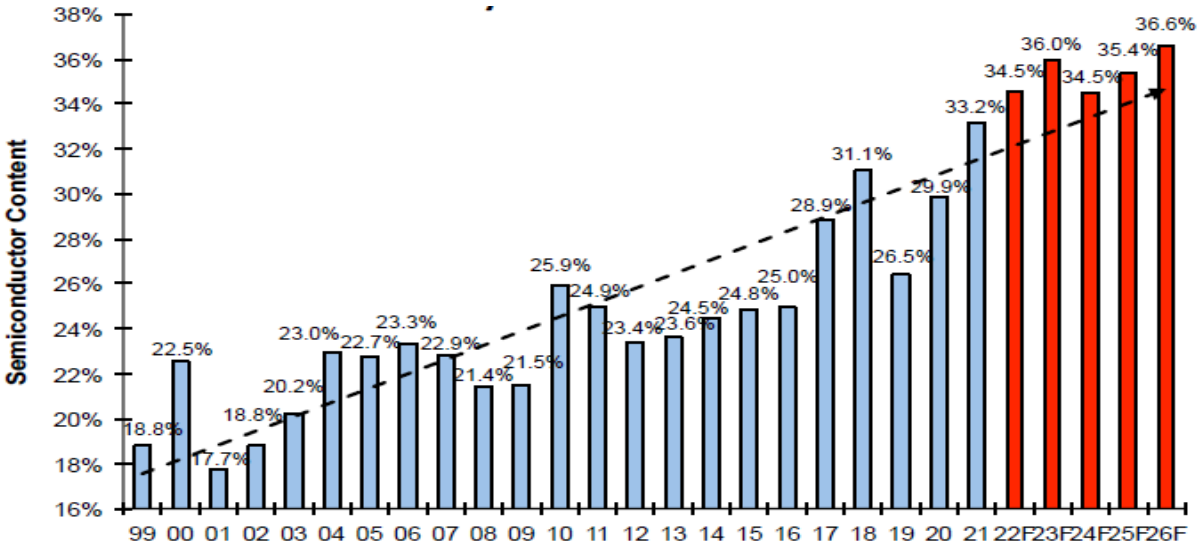

Figure 12. Semiconductor content in electronic systems (Source: IC Insights, ST, TI)

Market statistics related to regional shares of global semiconductor sales can be based on different types of data. In the estimation of regional shares and demand, one needs to consider that the value chain is complex, and before reaching its final destination, a semiconductor chip must go through a large number of process steps. The definition of the semiconductor market share therefore depends on which stage of the value chain one refers to, and it can be defined in at least three ways: by the **i) headquarter of the device maker**, ii) the **location of the customer to which the chips are shipped**, or iii) the **location of the end-user**, be it a business or a consumer (see Table 1). Recalling the example presented in Chapter 1: a microchip for a mobile phone can be designed in the US, manufactured in Taiwan, packaged in Malaysia, assembled on a board and in the final product in China, then the final product can be sold in Argentina.

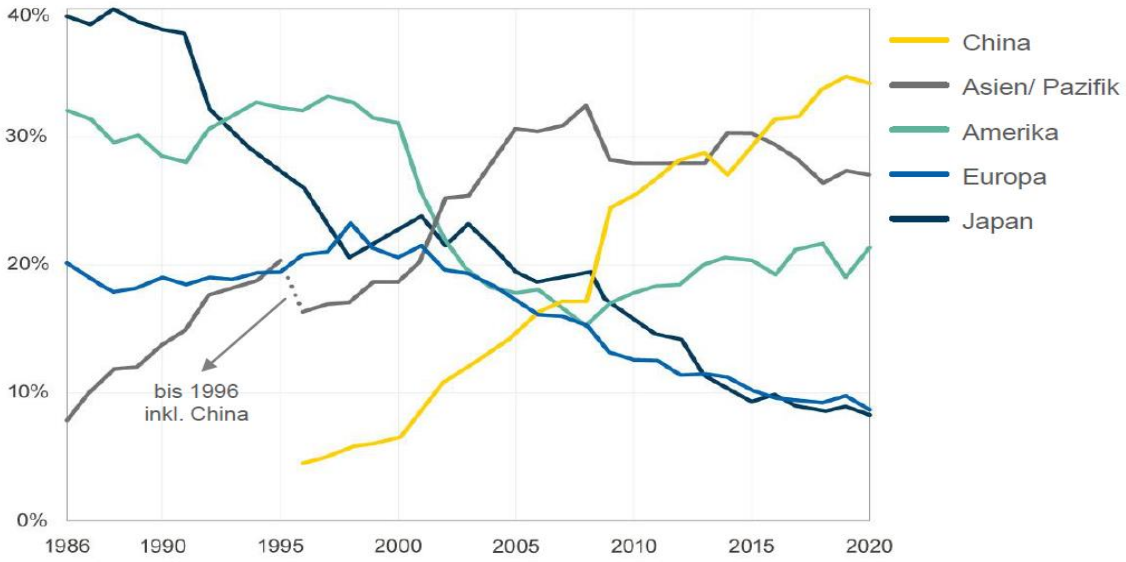

Figure 13. Global sales by headquarter location (Source: ZVEI)

i) **Market data related to value of production** of the various regions usually **report sales by headquarter of the device maker**, rather than the physical location of the production facility. In this context, the share of European headquartered companies is currently estimated to be around 9% (Figure 13).

ii) **Regional semiconductor demand usually considers the location to which chips are first shipped**, often for assembly in electronic boards and systems. In this context, the largest market in terms of regional sales is China, in view of the large number of systems assembled in that region. This is followed by Asia-Pacific, Americas and Europe, which represents a share estimated between 8.5% and 10%. (According to WSTS, sales in Europe in 2021 amounted to 8.6% of the global market, while for IBS Europe had over 10% of global demand).

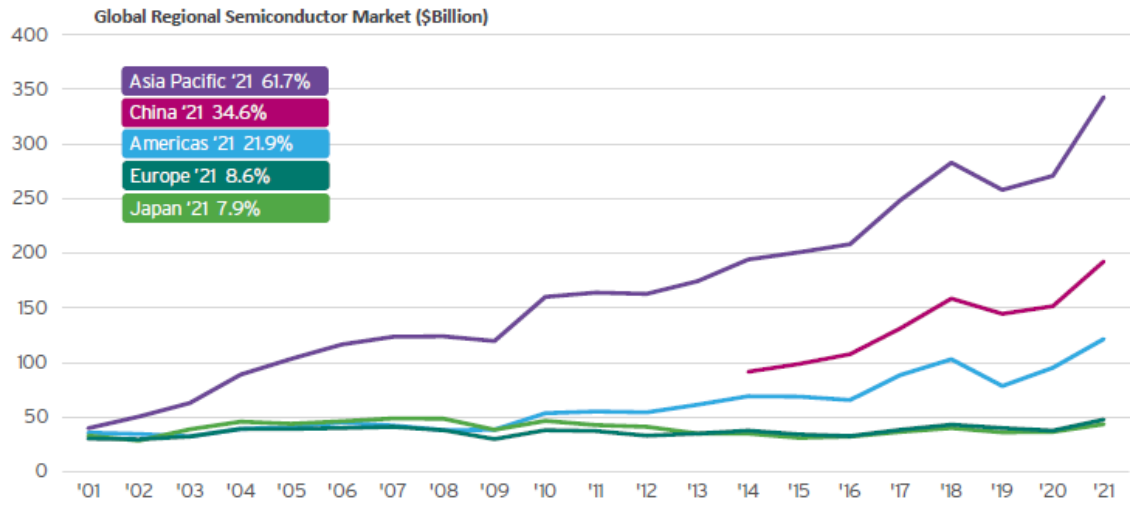

Figure 14. Regional sales for semiconductors (Source: SIA 2022)

iii) If we consider the **value of sales of end-user equipment and devices, Europe represents about 20% of the global market**, which is much higher than the regional share of global sales of components by European companies.

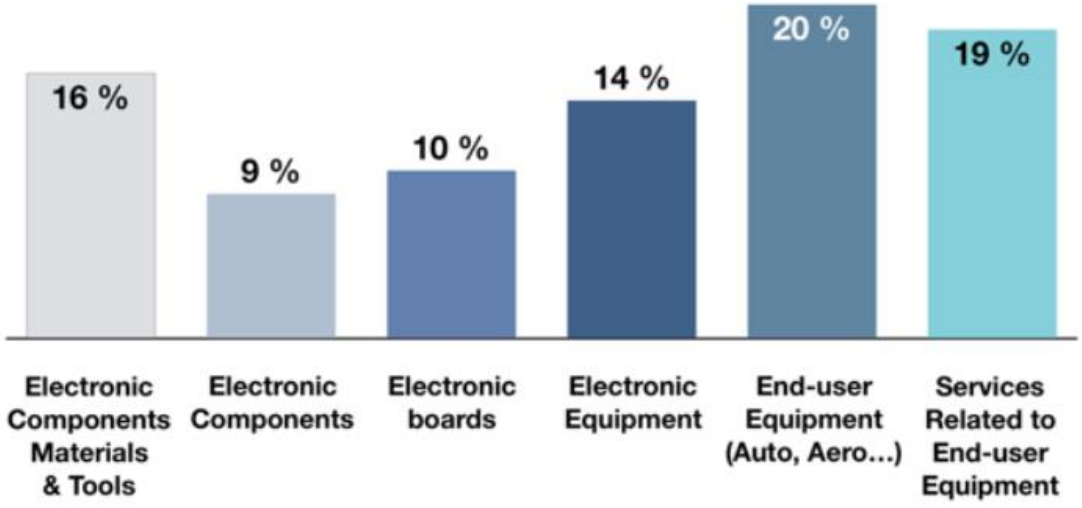

Figure 15. European share of global sales at the different steps of the value chain (DECISION[2], 2019)

[2] Study on the Electronics Ecosystem: Overview, Developments and Europe's Position in the World (EU 2018-19)

Summarised in Table 1, Europe's semiconductor market varies between approximately 10%, based on location of system manufacturer or system assembler, and 20% based on location of final end-user.

	By HQ location of the device maker	By location of device assembly	By location of device end-user
US	33%	19%	25%
China	26%	35%	24%
Europe	10%	10%	20%
Japan	10%	9%	6%
South Korea	11%	12%	2%
Taiwan	9%	15%	1%
Other	1%	<1%	22%

Table 1. Semiconductor sales by region as share of global total (BCG, SIA 2019)

From the above data it can also be inferred that the value of semiconductors that Europe produces is lower than the one it consumes. Indeed, as shown in Figure 16, in 2021 the EU exported semiconductors for a value of EUR 31.5 billion and imported for EUR 51 billion with a deficit of EUR 19.5 billion. Top export destinations and import origins are countries with major activities in wafer fabrication, and chip packaging, test and assembly: China, Malaysia, Taiwan and the USA.

Although the current level of consumption of semiconductor components in Europe cannot be directly compared to the lower value of components produced by European companies (or the value of components produced in the EU), it provides an indication supporting **Europe's ambition to increase its level of sales or of local production, taking into account that the increase in demand will also lead to an increase in exports.**

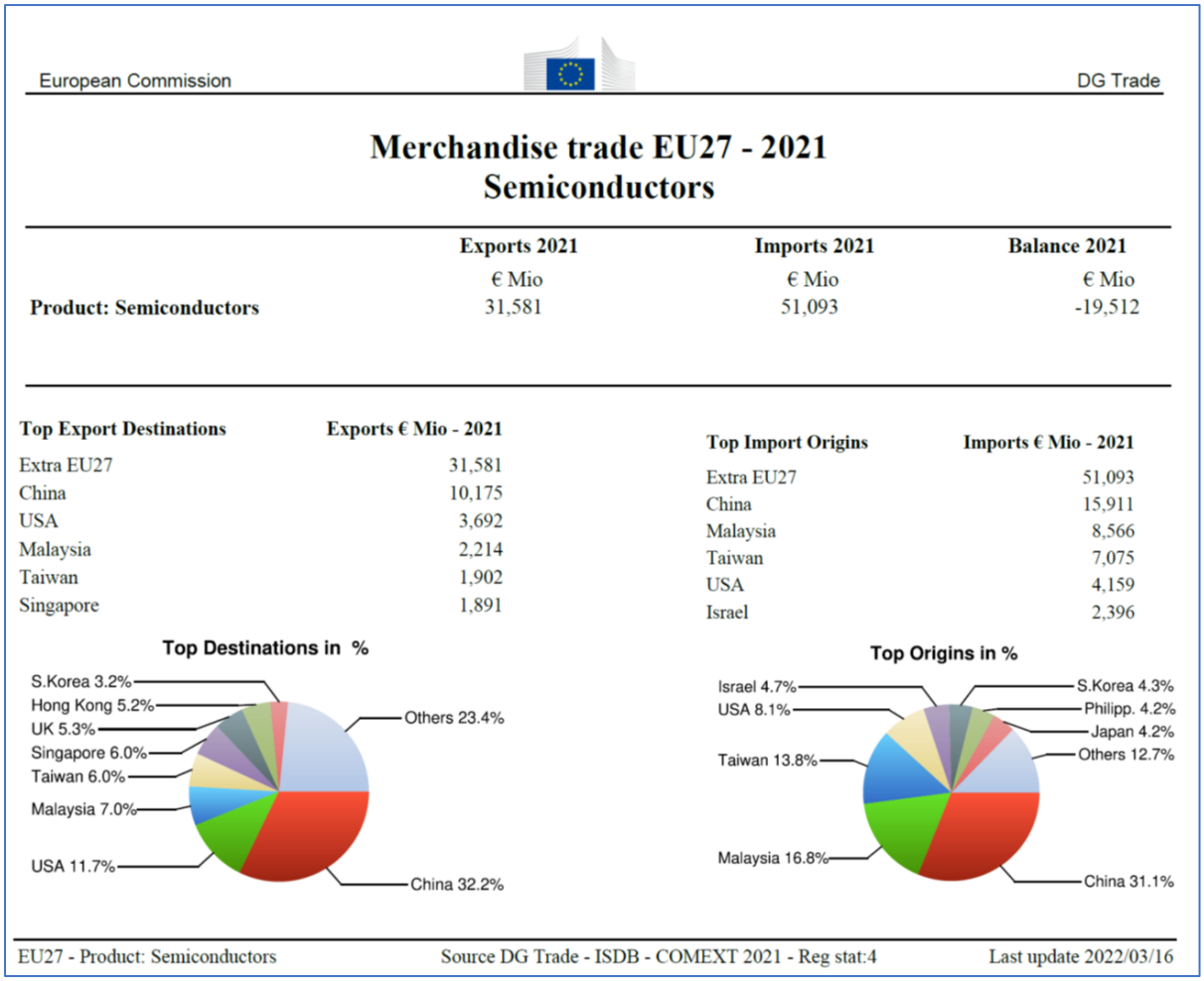

Figure 16. EU semiconductor import/export in 2021 (source: European Commission, ISDB, Comext)

As it has been mentioned in previous chapters, the fabrication of semiconductor chips is concentrated in Asia. Figure 17 shows the major foundries and their respective market shares. Taiwan is a major player in the semiconductor industry with 65% of foundry revenues; **TSMC has a 53% share of the global semiconductor foundry market**. The next largest foundry is Korea's Samsung with a market share of 17.1%. Other leading foundries include UMC in Taiwan, SMIC in China and the US-headquartered GlobalFoundries.

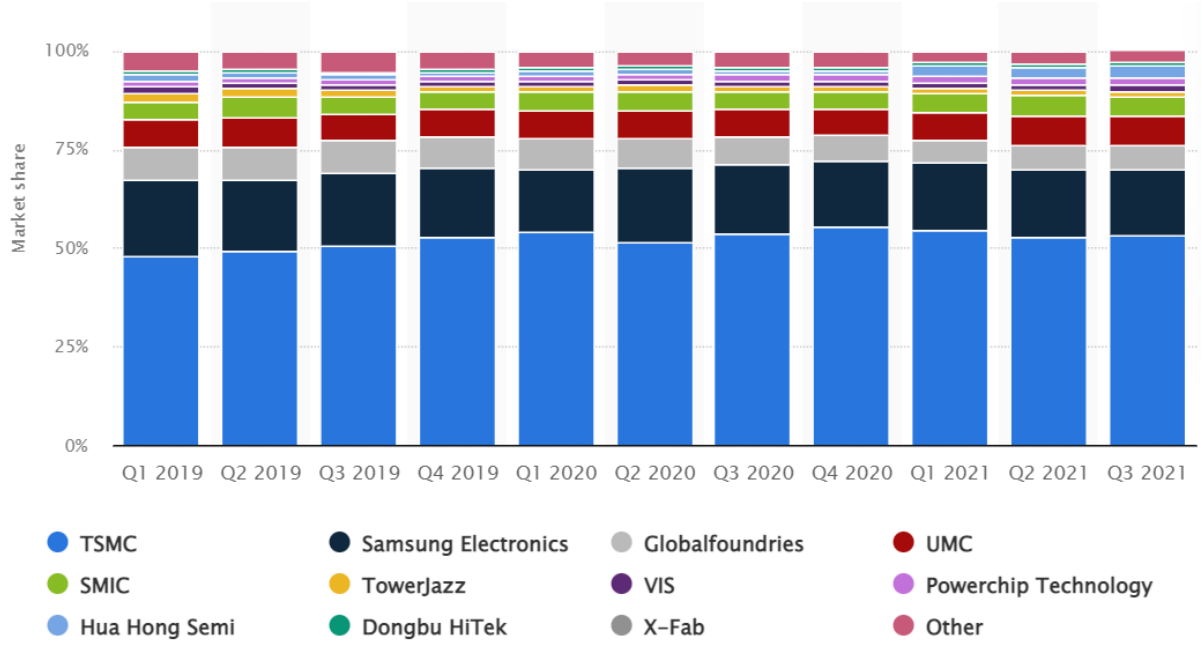

Figure 17. Global Foundry Market Share of Semiconductor Production 2019-2021 (Source: Statista, Trendforce)

TSMC and Samsung[3] are the only foundries currently capable of manufacturing chips below 10 nm. Although demand for mature nodes will continue, future growth is expected to be concentrated mostly in the most advanced nodes (see figure 18).

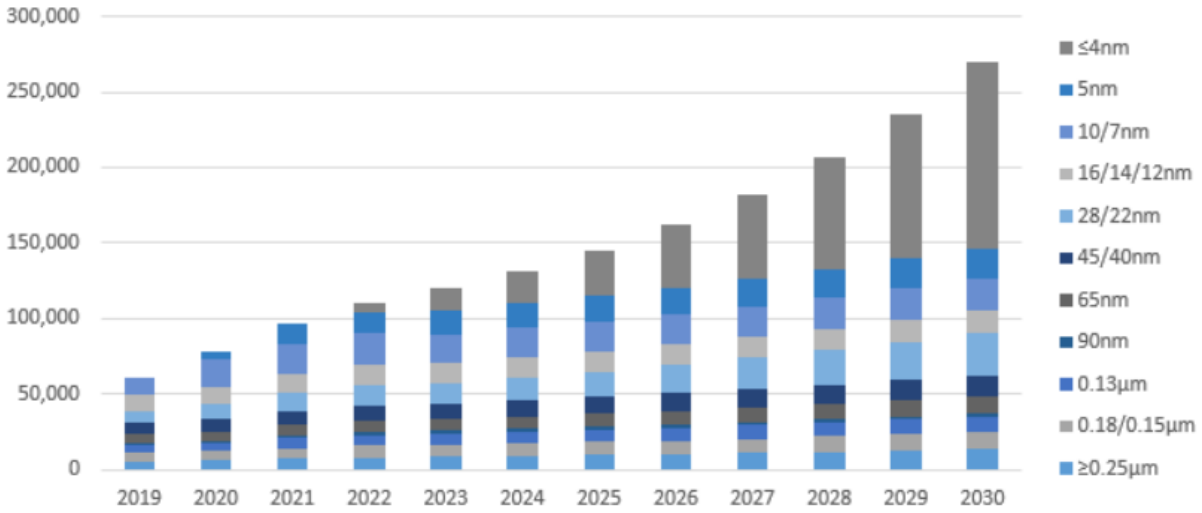

Figure 18. Foundry Market Growth Areas by node (Source: IBS 2022)

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Concerning **the level of production of fabs** located in the various regions, usually this is only estimated in terms of number of wafers, not in terms of value as this varies considerably based on different factors. In this respect - see Figure 19 - Europe has observed in the last 20 years a gradually declining share of

[3] Intel, which is planning to catch up with TSMC and Samsung in leading-edge nodes, recently announced the intention to start providing foundry services to third parties
https://www.intel.com/content/www/us/en/foundry/intel-foundry-services.html

global capacity to 9.4%, as its investments have remained nearly constant in the past years, versus an overall increase of costs of new production facilities. **The majority of capacity in Europe is still concentrated at 180 nm and above** (see fig 20). The only capacity below 20 nm is at Intel in Ireland (14nm).

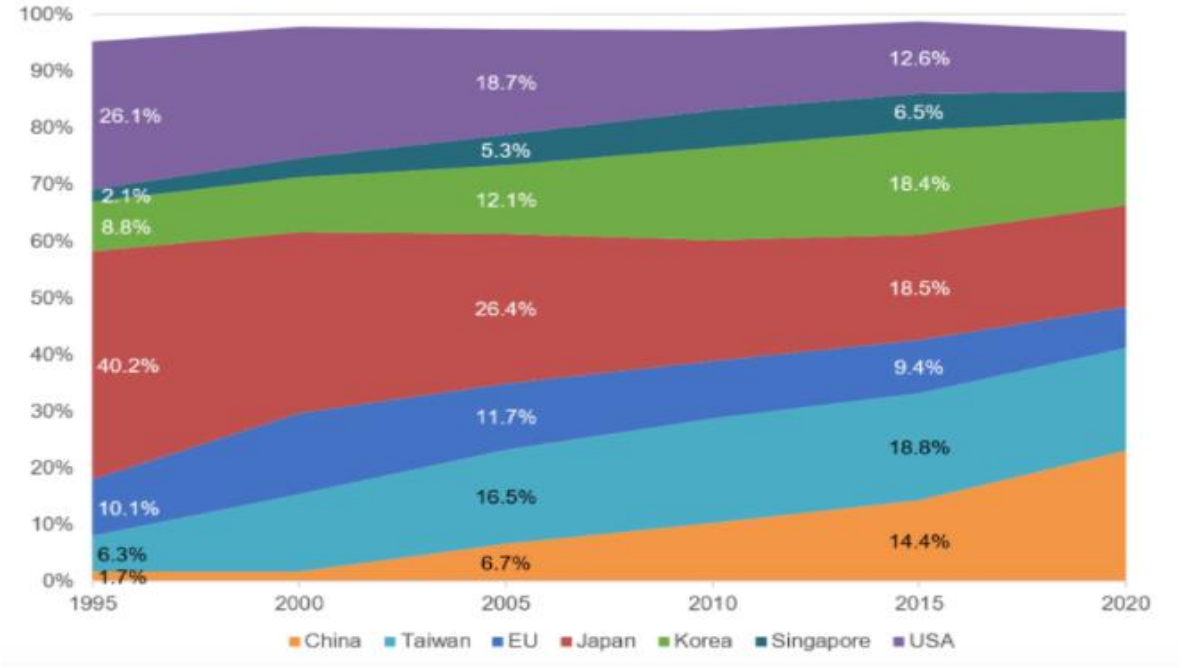


Figure 19. Wafer capacity by region in 200mm equivalent 1995-2020 (Source: ESIA, SEMI, 2021)

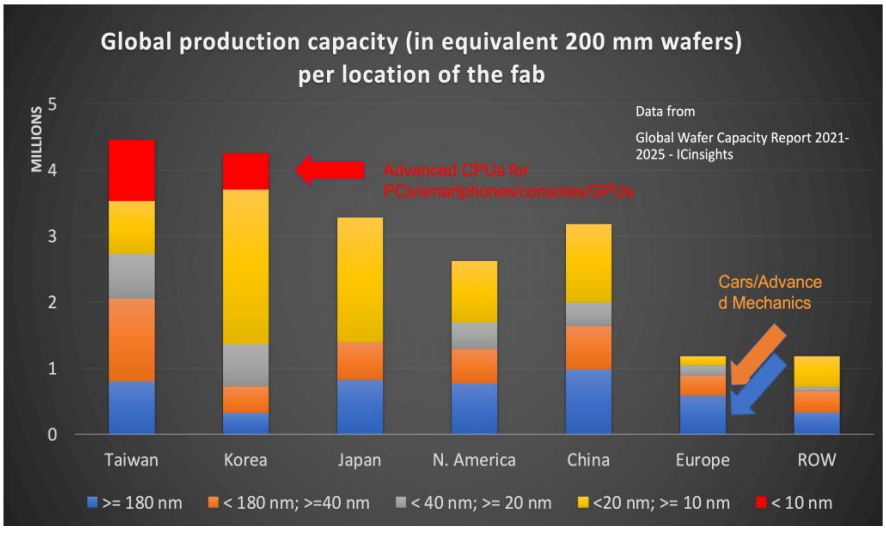


Figure 20. Wafer capacity by geographic region and node type (Source: IC Insights, 2021)

The predicted worldwide **market growth for semiconductors in key application markets** over the present decade is shown in Figure 21. Chips for **automotive represents the highest growth market,** forecast to grow by more than three times its current value by 2030. Demand for devices for servers, data centres and storage will also rise significantly as the data economy grows. It is expected that there will be a **doubling of chip demand for both the industrial electronics and consumer electronics markets**. The smartphone market is expected to nearly double by 2030. Personal computing demands

will continue to rise, but more slowly, having already grown significantly during the COVID-19 pandemic.

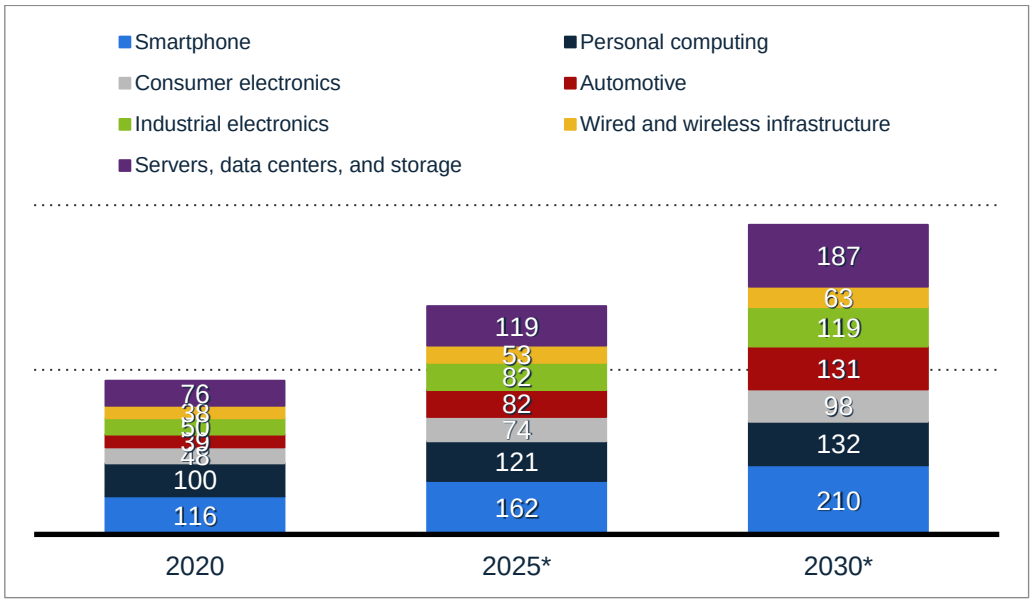


Figure 21. Semiconductor Market Size forecast by application (in USD billion, Source: Statista, ASML 2021)

3.2 Market Position of Europe

As shown in Figure 21, the bulk of global demand (close to 70%) comes today from end-use applications in **computing** (including PCs and data centre infrastructure) and **communications** (including smartphones and network infrastructure). In view of their centrality to digital transition, Europe's share of these markets is quite small.

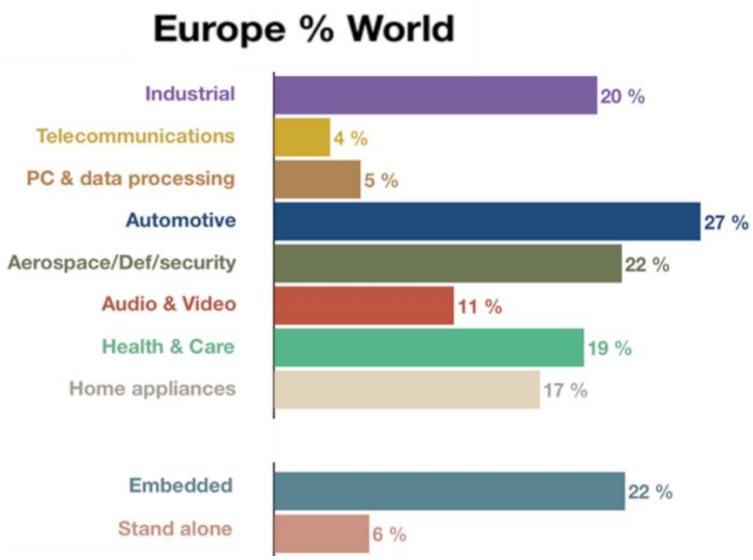


Figure 22. Production of electronic systems in Europe as share of global sales (Source: Decision, 2019)

Europe has a strong position in components for embedded and professional systems, which reflects its strengths in the production of electronic systems, as shown in figure 22, whereas little presence is left today in the Union in the area of computers (personal or for data centres) or mobile communication devices. This is reflected also in the European demand for semiconductors from different market segments, which, as shown in figure 23, is particularly high in automotive and industrial automation,

segments previously ruled by analogue and mechanical technology. European players such Infineon, NXP, STMicroelectronics and Bosch are indeed among the global leaders in these markets for which the expected growth rate is highest in the coming years (see section 3.3).

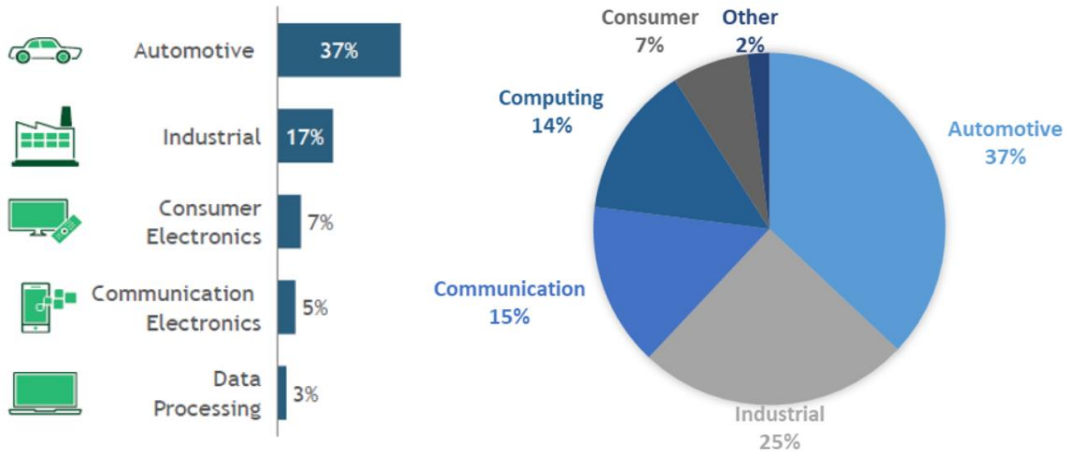


Figure 23. European share of semiconductor market segments, and demand by end market (Sources: Decision, ZVEI, 2019)

In addition to these market segments, Europe is relatively strong in the smaller but growing healthcare, wireless (5G/6G) networks, and aerospace and defence segments. These markets are described in Chapter 4.

3.3 European Strengths in the Global Market that can be Built Upon

3.3.1 A snapshot of the European supply chain

In terms of role in the various stages of the value chain, Europe has core strengths in R&D as well as in the supply of advanced material and especially of manufacturing equipment. However, in some key stages of the supply chain from design and IP to front-end and back-end manufacturing, the EU needs to address gaps and dependencies from other regions.

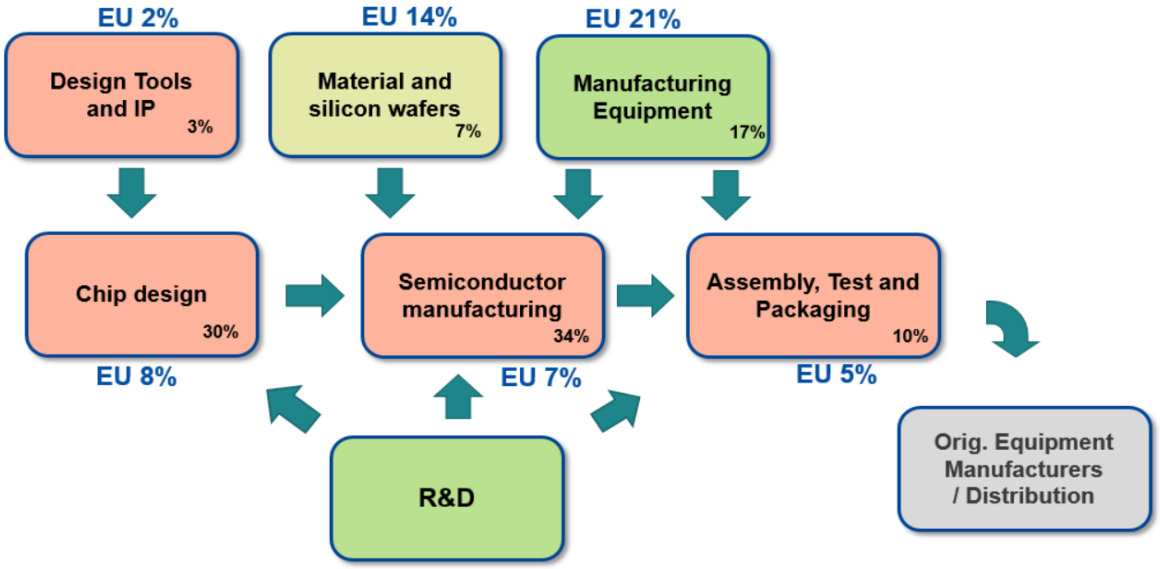


Figure 24. The main segments of the semiconductor supply chain with relative added value and EU market share (Sources: European Commission, CSET, IC Insights, BCG/SIA, SEMI)

As set out in Chapter 1, the semiconductor manufacturing value chain is reliant on a wide range of specialist materials, chemicals and sophisticated equipment provided by vendors across the world. Within this global supply chain Europe has world-leading suppliers of **equipment**, e.g. ASML, EV Group, ASM International, and **raw materials providers**, such as Siltronic, SOITEC, BASF, Linde, Merck KGaA and Air Liquide, providing **wafers** and **gases**[4]. In some cases, the global supply chain for advanced chips is totally reliant on European manufacturing equipment such as EUV lithography machines from ASML (see Figure 24).

Figure 25. Advanced Lithography Machine form ASML Enabling Production of Leading-Edge Chips

Europe also has leading **chipmakers specialised in the automotive and industrial automation markets**, accounting for about 40% and 20% respectively of the total semiconductor market in those segments (see Figure 25).

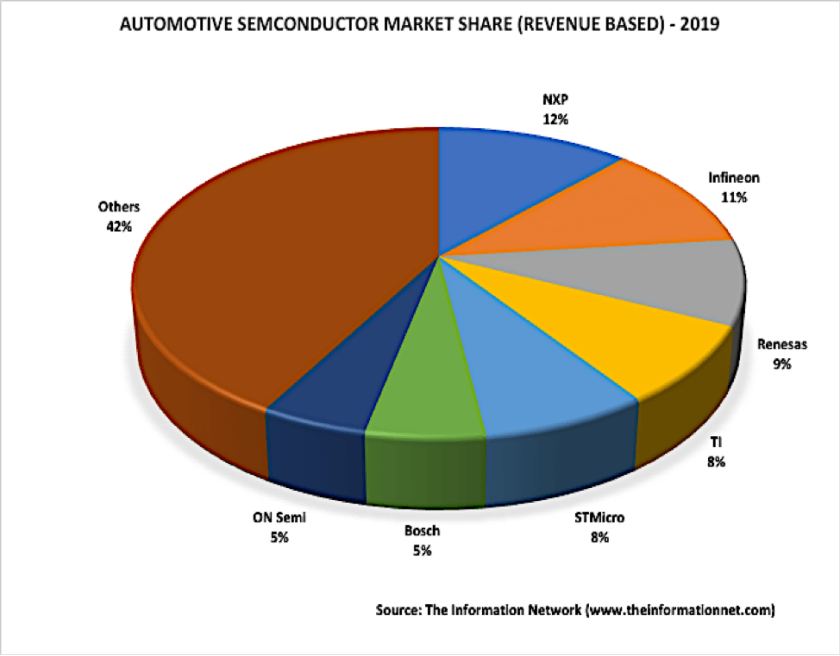


Figure 26. Automotive Semiconductor Share

In **automotive,** NXP and Infineon are in the top 2 positions globally; ST and Bosch are also strong players.

[4] Europe is dependent on third countries for certain materials, such as photoresist and silicon metal.

European companies dominate the market for embedded **security chips**, the leading actors being NXP, Infineon, ST, Gemalto and Idemia. The concept of trusted chips is regaining traction as cyberattacks grow in number and sophistication, threatening data privacy and security, and the safety of digital systems including cars, trains, planes and physical networks (see Chapter 5.3).

3.3.2 Design and Manufacturing in Europe

In Europe there are over 50 semiconductor fabs located in many different Member States, including Germany, France, Ireland, Italy, Austria, Netherlands, Belgium, Hungary, Czech Republic, and Sweden. The majority of these fabs produce at mature nodes on 150 mm and 200 mm wafers; only a limited number of fabs process 300 mm wafers, such as the ones from Intel in Leixlip (IE) (producing at nodes down to 14 nm), GlobalFoundries in Dresden (DE) (down to 22 nm), ST Microelectronics in Crolles (F) (down to 28 nm). New analogue fabs have recently opened, such as the one from Bosch in Dresden (DE), Infineon in Villach (AT) and ST Microelectronics in Agrate (IT).

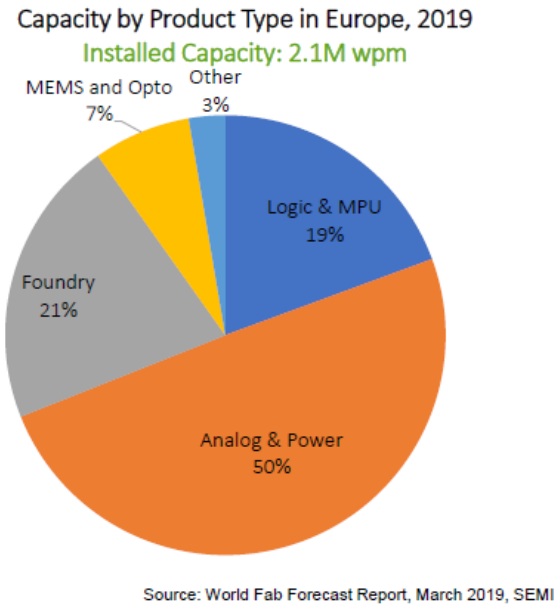


Figure 27. Global Production Capacity and Product Types in Europe

Europe's capacity to design chips resides largely with its IDMs and is linked to the markets where they are strong today. However, few chips are designed today without US-origin IP. European chipmakers using US-origin IP have to apply for licences to export to Chinese companies; this can have a negative impact on trade and market share. Europe's share of fabless design has declined from 4% in 2010 to less than 1% today[5]. The fact that there are no EU companies in the top 50 is a matter of concern, not least because among the various segments of the semiconductor value chain, design generates a large share (over 30%) of the value of the final product. Supporting the expansion of design capabilities and the growth of fabless companies in the EU is therefore of critical importance.

Europe has a vibrant ecosystem of SMEs and start-ups spread across many EU Member States. Difficulties in accessing equity however limits their growth prospects. In general companies producing

[5] Source IC Insights (https://anysilicon.com/fabless-company-sales-by-region-2018/). Note that Dialog (UK) has been acquired by Renesas (JP) in 2021.

hardware have more difficulty financing through the "Valley of Death" from demonstration-scale to commercialisation than those producing software as they are founded upon engineering innovation and/or scientific advances (which makes them inherently more risky)[6].

3.3.3 The Research efforts of Europe

Research activities in semiconductors include:

- **basic research**, which studies materials and processes stimulating innovations in performance and efficiency, and that is carried out mostly by academia and research organisations, sometimes in cooperation with industry;
- **applied research**, studying the effect of the basic principles in specific fields of application, where still research and technology organisations are quite active, but industry plays also key role;
- **development**, which puts the learned principles into practice in terms of devices of manufacturing processes, and is mostly responsibility of the industry itself.

If one considers the average investments that the EU semiconductor industry makes in the 3 steps above, overall they exceed 14% of global sales, which is one of the highest of all industries. At European level, collaborative and individual research efforts in semiconductors are generally supported by the Union's Research and Innovation Framework Programmes, as well as private-public partnerships or joint undertakings (JUs) such as the Key Digital Technologies (KDT) JU (now proposed to become the Chips JU). Further, Member States can support R&D projects by undertakings, up to first industrial deployment, in the framework of an Important Project of Common European Interest (IPCEI), such as the one on Microelectronics and Communication technologies, recently pre-notified to the Commission (see also section 8.1.8).

The strategic alignment between the European Commission, Member States, industry, research and technology organisations (RTOs) and universities, through the ECSEL JU and its predecessors, has encouraged the pooling of European industry-driven R&D efforts. Between 2014 and 2020, under the ECSEL JU, an investment of EUR 2.4 billion (shared equally between the Commission and Member States) was matched by industry, RTOs and universities. This approach has been instrumental in the development of various technologies that have been successful on the market.

Over the years the JUs have supported and developed key innovations in CMOS, mixed-signal, sensor, and power technologies as well as Fully Depleted Silicon on Insulator (FDSOI) semiconductor process technology (see Annex 4), new lithographic techniques such as EUV, and has strengthened the semiconductor equipment and materials ecosystem in Europe.

Underpinning this, there is a large RTO community with world-leading actors, represented among others by IMEC (BE), CEA-LETI (FR), Fraunhofer Group (DE), VTT (FI), TNO (NL), CNR (IT), Tyndall (IE), AIT (AT), RISE (SE), CSIC (ES), INESC (PT), FORTH (GR), CNRS (FR). This is complemented by leading technical Universities, including the ones of Delft (NL), Eindhoven (NL), Grenoble (FR), Dresden (DE), Leuven (BE), Graz (AT), Milano (IT), Tampere (FI), Cork (IE), Bratislava (SK), Lund (SE), DTU (DK), Brno (CZ), Gdansk (PL), Thessaloniki (GR), Bucharest (RO), etc. These and many others across Europe contribute to advances in the field, developing European IP, hosting pilot lines and contributing to skills development and training.

[6] Financing Europe's Digital Transformation: Unlocking the value of photonics and micro-electronics, EIB, June 2018

Despite the important results in R&D achieved through the above efforts, the EU is much less successful in translating results into industrial benefits. The first Important Project of Common European Interest (IPCEI) on Microelectronics - originally approved in December 2018 with France, Germany, Italy and the UK, with Austria having joined in 2021 -granted aid of up to EUR 1.9 billion to upstream component manufacturers to carry out R&D&I and First Industrial Deployment[7] (FID) in the EU to support applications in downstream industries. It played a role in leveraging industrial investments in Europe of more than EUR 6.5 billion including the first greenfield investment in a fab in Europe in more than a decade (Bosch in Dresden - see Chapter 8), and brought together 32 participants (mostly companies). This has without doubt added value to above-mentioned developments supported by the JUs.

The JUs - being largely bottom-up in nature[8] - have tended to be more closely aligned to the core business interests of the industry. There has been less emphasis on addressing gaps and emerging needs at European level, such as the ones related to the digital transition (including a focus on logic and memory), with end-user companies playing a more active role[9]. The successor JU to ECSEL - the Key Digital Technologies JU – allows also for a top-down approach, whereby part of the funding is allocated in advance to topics selected by the public authorities and the industry partners of the JU. As alluded to in section 3.3.2, an important concern is the lack of venture capital funding in the sector that limits the ability of Europe's most innovative deep-tech start-ups and SMEs in this sector to translate new innovations into products.

The measures proposed to address the above issues are outlined in section 8.1. In the following chapters (4 and 5) the opportunities for innovation in Europe are highlighted.

[7] First industrial deployment means the upscaling of pilot facilities, demonstration plants or of the first-in-kind equipment and facilities covering the steps subsequent to the pilot line including the testing phase and bringing batch production to scale, but not mass production or commercial activities (see Communication C/2021/8481), OJ C 528, 30.12.2021, p. 10–18, paragraph 25).

[8] In particular, the JUs have until 2020 based their workprogrammes on a broad Strategic Research and Innovation Agenda put together and regularly updated by industry associations.

[9] See for example, Study on the impact of ECSEL funded actions, Final Report, Deloitte.VVA, February 2020 or ECSEL Book of Projects volumes 1, 2 and 3. While not providing in-depth analyses, clearly the majority of products are aimed at reinforcing strengths in semiconductor markets or technologies where EU industry is already well-positioned. There is also relatively weak participation by the EU's major end-users of semiconductors. Steps have been taken in the last two years of ECSEL to bring semiconductor suppliers and end-users together in projects in a "full value-chain approach".

4. Technology Trends and Evolving User Requirements for Key European Sectors

4.1 Industrial Automation

With 20% of market share in industrial electronics, Europe is ranked second after China, but ahead of the US. The global market for industrial control and factory automation is predicted to grow to almost EUR 140 billion in 2022.[10]

Wider use of digitalisation and automation is currently modernising both manufacturing and supply chain management. There is a clear trend for intelligence to migrate closer to machinery and processes in a factory to carry out inspection tasks or for predictive maintenance. This requires a range of processing capabilities at the edge[11] of the network with a wide range of connected devices and systems, the so-called Industrial Internet of Things (I-IoT).

Industrial robotics is also evolving, enhanced by edge computing capabilities. There is increasing interest in modular self-reconfiguring robotics to perform different tasks, and in robots able to interact and collaborate with humans to take over the mundane or dangerous tasks (the so-called "cobots").

A key concern is the reliability of these new IoT components. In particular if they are performing control tasks (in addition to computing tasks) they may also cause shutdowns. **This requires technological resilience against cyber threats which is pushing demand for secure edge computing components.** Factory owners are also concerned about sensitive data being sent to remote data centres and the cloud, so local on-premise clouds are often used.

The Industrial Automation domain is being revolutionised notably by the Internet of Things, requiring powerful secure edge computing devices and high rate, low latency communications such as those provided by 5G.

Looking to the future, there are drivers towards scalable, reconfigurable and flexible first-time right manufacturing with zero-downtime precision manufacturing, including predictive quality and non-destructive inspection methods. **This is driving advances in the application of Artificial Intelligence not only at the local level, but also for global optimisation.[12]**

The development of Digital Twins allows for the evaluation of industrial assets at all factory levels, and over system or product life cycles. This requires significant processing and also data gathering across the factory from sensors and equipment, possibly enabled by dense 5G interconnectivity.

There will also be increasing interaction with an augmented workforce via wireless and mobile technologies in shopfloor automation and information management to support more flexible, modular and remote operation of manufacturing assets. The integration of 6G wireless tactile networking capabilities coupled with advanced embedded computing intelligence platforms will play a central role in the realisation of next generation digital manufacturing workplaces.

[10] Thompson, H., Reimann, M. Et al. (2018). Platforms4CPS. Key Outcomes and Recommendations.
[11] The term "edge computing" refers to computing or data processing close to where the data in question is gathered or generated. It is in contrast to centralised computing where the data is transmitted to a data centre or the cloud for processing. Edge computing has become possible due to the variety of increasingly powerful processor chips (GPUs, TPUs, …) that can be embedded with cameras or sensor devices that capture the data.
[12] Industrial IoT Edge 4.0 Framework: A Gamechanger | ARC Advisory (arcweb.com)

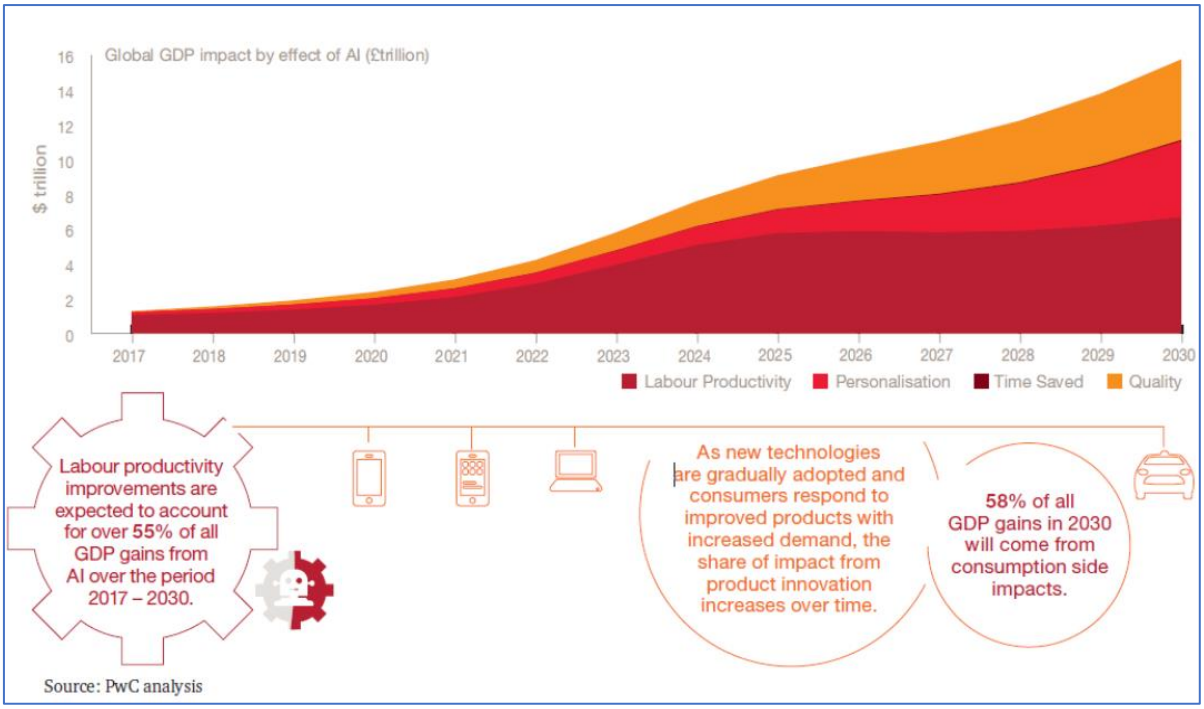


Figure 28. Growing Use of AI in Manufacturing Optimisation and Products (Source: PwC)

Sustainable production is also a key driver and companies are striving towards an optimised materials economy to reduce raw materials used, energy and chemical usage, and scrap, as well as a move to circular manufacturing models over the lifetime of products to improve recycling and reuse.

To support the demanding requirements for robotics and automation as well as the increased application of AI at the edge for factory optimisation, there is a need for advanced semiconductor technologies, such as: leading-edge processors (e.g. 10 nm and below), advanced packaging of chiplets and heterogeneous integration to combine sensing, processing, AI acceleration and wireless communication in a single package.

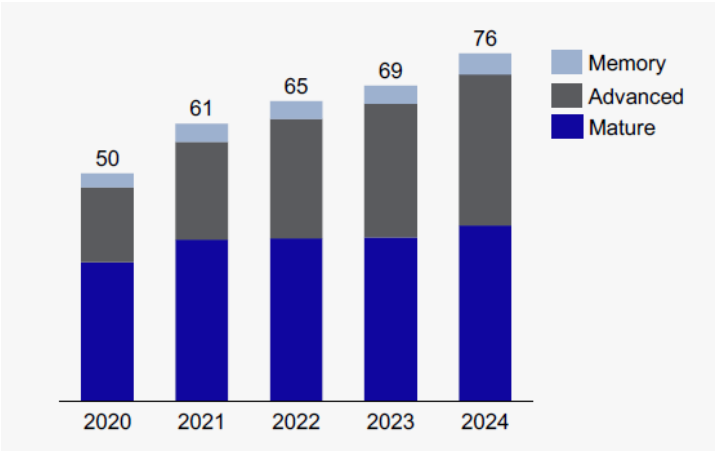


Figure 29. Semiconductor market evolution for industrial electronics, in USD billion (ASML)

4.2 Automotive Industry

According to various analysts, the automotive segment is the one with the highest expected growth in the coming years, with a CAGR estimated between 11% and 15%. According to IBS, by 2030, the market may be worth USD 113 billion, with 39% of fully electric vehicles (EV) sold worldwide, and the wide majority featuring a high level of automation (L4 or L5).

In a modern car, there are around 1500 semiconductors with an average value of USD 500 exploiting a range of fabrication processes. By 2030, this number is expected to rise to 3000 semiconductors with an average value of USD 1200.[13] This includes a wide range of components such as microcontrollers, microprocessors, fusion processors, Systems on a Chip (SoCs), ASICs, memory, display drivers, sensors, analogue and power electronics.

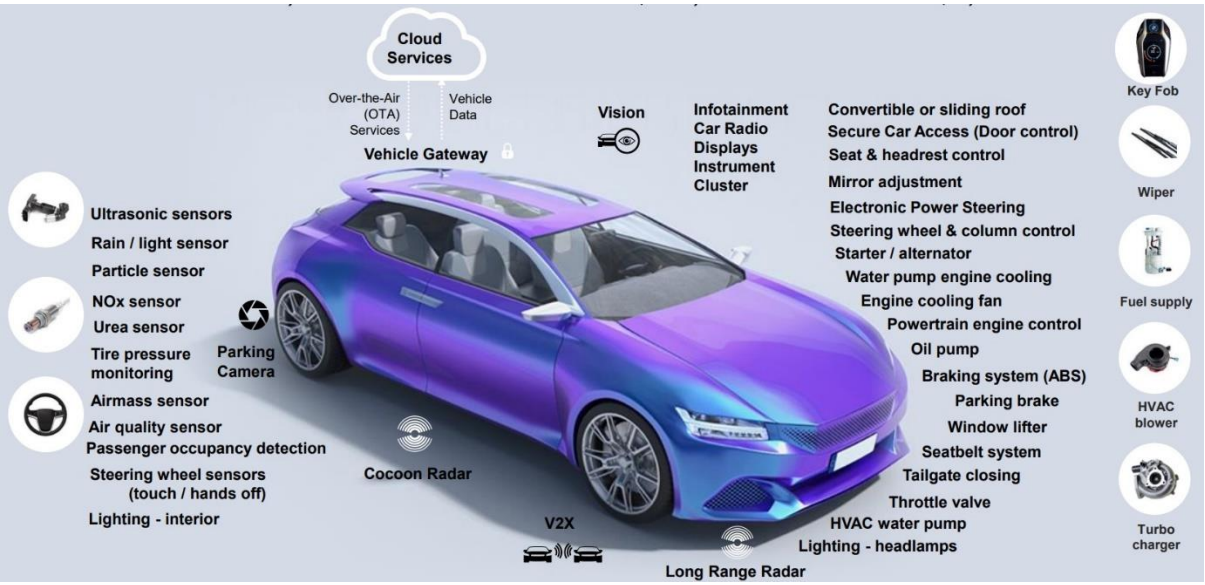


Figure 30. Components in modern car systems (Source: NXP CMI)

The range of technologies required currently varies from 16 nm devices for radar processors and for networking, 40nm devices for processors in general, 65-350 nm devices for mixed signal devices, LED, bus and sensors, and 1µm devices for power electronics. In view of the shift towards higher level of automation, with processors for sensor fusion, on-board computing and communication, demand for chips produced at more advanced nodes is expected to grow in the coming years.

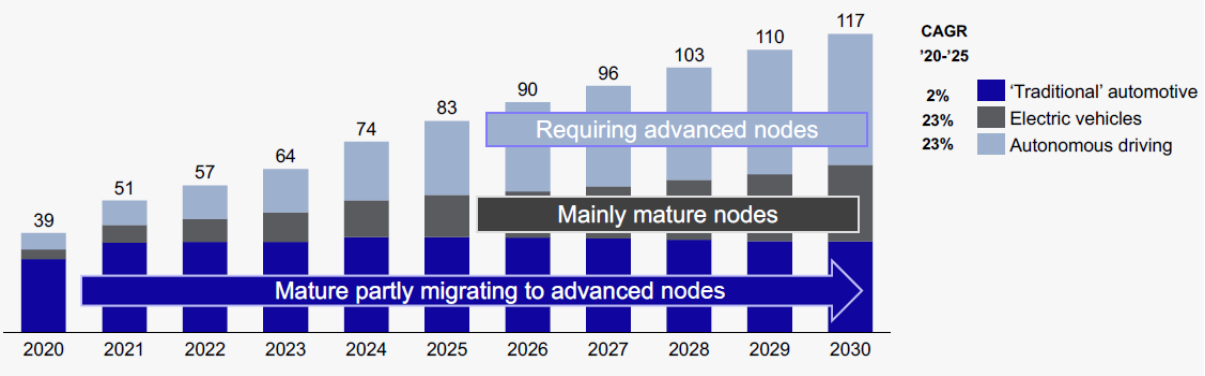


Figure 31. Semiconductor market evolution for automotive chips, in USD billion (Source: ASML, Gartner 2022)

There are three key drivers in the automotive sector which are increasing the use of semiconductor devices: **connectivity for safety and infotainment systems, increased automation levels and the move towards electric vehicles**.

[13] IBS, 2021

Type of Semiconductor	Volume Node(s) today	Design node for new products	Company	# per average vehicle (2019)
Auto SoC's	65nm - 28nm	16nm (ramp 2021) 5nm design (SOP2025)		9
	65nm – 28nm	16nm ramp 2020		
	28nm – 7nm	5nm design		
	40nm – 28nm	7nm design		
Auto Memory	55nm – 40nm	Not announced		13
	18nm – 15nm	~10nm		
Auto MCU	180nm – 55nm	40nm ramp 2021		34
	180nm – 40nm	40nm & 28nm		
Analog (Linear) & Power Semiconductors	130nm & larger	90nm		253
Discretes / Small Signal Transistors	130nm & larger			406
Sensors	130nm & larger			45
All other types	90nm & larger			213
Total				960

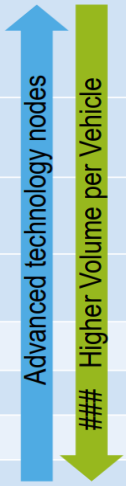


Figure 32. Predominant Technology Nodes per Product Type (Source: Strategy Analytics, Jan'2021 for 2019 figures, Company reports)

Although the number of cars being produced has reduced significantly from 95 million in 2017 to 75 million in 2021 as a result of the current supply crisis, **the number of chips required per car has gone up dramatically driven by new features and the move to hybrid and electric cars**. In order to ease the management of such a large number of components, there is a trend in the industry towards more centralised architectures and the use of System on Chips (SoC), requiring high-performance processors. Further, the increasing penetration of electric mobility will lead to a high growth for power electronics components, especially those adopting compound substrate technologies such as Silicon Carbide (SiC) for fast charging and inverter control[14].

Other areas of device usage are increasing very rapidly. **A concern is in the use of analogue chips as they are key components across a wide range of applications.** This includes SoCs, signal conditioning for sensors, bus transceivers, drives for motors, LEDs, displays and radar transceivers, audio and RF systems. **The lead time for analogue devices is still increasing and this is likely to limit production in the future**[15]. Here there is competing demand for fabrication resources from other sectors such as phones, high-end audio and contactless payment.

In the automotive sector the requirements for connectivity, infotainment, increased automation and electric vehicles are leading to a radical increase in demand for digital and analogue components which is becoming increasingly hard to meet.

4.3 Healthcare

Any medical device used in hospitals and doctor practices that is powered by electricity grid or batteries, depends on semiconductor components to operate. This includes life-saving devices such as defibrillators, pacemakers, insulin pumps, ICU equipment or diagnostic machines such as MRI or CT scanners, ultrasound, ECG stations. As the population ages and the cost of healthcare increases,

[14] According to Yole, the SiC device market is expected to grow at 34% CAGR, from beyond US$1 billion in 2021 to over US$6 billion by 2027 (http://www.yole.fr/Power_SiC_March2022.aspx)
[15] Source IHS Markit™

healthcare is becoming more decentralised, personalised and focused on prevention. **Although there are large differences in healthcare spending across EU Member States, the average figure is approximately 10% of the EU's GDP, or EUR 1.6 trillion**. Solutions for remote monitoring, telemedicine and digital health in general will become imperative, particularly for elder people with chronic diseases allowing them to remain in their own homes and reduce costs of care. These include wearable and implantable devices to provide remote monitoring and alerts for carers, or under-the-skin drug delivery systems, which will drive up the volume for this market segment. The boundaries between medical technologies, medicinal products, digital health technologies and the semiconductor industry are disappearing, resulting in new diagnosis and treatment solutions. This requires digital processing, advanced electronic sensors and photonics, MEMS, and high volume, high-quality, low-cost production capabilities. There is therefore an incredible potential for growth in this segment.

The medical device end-use market is currently estimated being about 1.3% of the total semiconductors market (source Omdia, 2020), around USD 7 billion. Therefore demand may be viewed as limited, but especially very fragmented, which is one of the key obstacles for growth. There are more than 25,000 SMEs in Europe active in the field of medical devices – many spun-out from RTOs and academia. However, only very few breakthrough innovations reach the patient or the clinic. **A key barrier is that these specialised devices are needed in small numbers, which is at odds with foundries' expectation of large volumes to amortise production costs**. There is also a lack of open technology platforms in the medical device industry. Some **European companies (including Philips) are cooperating to develop technology platforms that are open to other parties for bioelectronic medicines** thus giving potential for viable production volumes to be achieved[16].

Due to the low production volumes and specialised nature of devices required in the health sector, there is a need to develop industry standard platforms that can be used across the community and to introduce measures for the security of supply to the medtech industry.

4.4 5G and 6G Communications

Communication is together with computing the largest segment of the semiconductor market, with revenues in the order of USD 200 billion. Over 90% of the market is wireless communication, mostly due to the 1.5 billion of mobile handsets sold on a yearly basis. This market currently drives the 'More Moore' trend of scaling in chipsets, with smartphone brands having the largest volumes, necessary to justify the costs of new 3 nm and planned 2 nm fabs. 5G, the fifth generation of standard for mobile communication technology, provides far higher data rates (20Gbps versus 150mbps), with lower latency (1ms vs 60ms on 4G LTE) than previous generation 4G LTE, and the ability to connect more devices in a given volume. Semiconductor consumption of a 5G smartphone is at least 1.4 higher than the previous generation, and the market value of 5G chipset sold is already surpassing the value of chipsets for smartphones up to 4G. 5G has many potential applications, going beyond mobile phones, notably in industrial automation and in automotive.

Another important subpart of this segment is related to chipsets for wireless communication infrastructures, a smaller but highly strategic market, requiring high-performance components. Europe is strong in infrastructure equipment, with two market leaders as Ericsson and Nokia, but companies from US and China have taken the lead in terms of chipsets. Further, the market is evolving towards disaggregation of hardware and software, with open standard interfaces, and virtualised, cloud-based

[16] POSITION-2. The next generation smart catheters and implants.

management of the network. This is disrupting the current business models and the established positions, with geopolitics playing also an important role in the adoption of specific technologies.

The next generation communications technology 6G is also being developed for targeted introduction in 2030. In 6G very high frequencies are utilised which will give very high data transmission rates with little or no latency, more heterogeneity and increased sensitivity to the environment. It will support decentralised models with automated management, employing pervasive edge AI, blockchain technologies, virtual reality and augmented reality, which can open up new applications such as the "metaverse"[17]

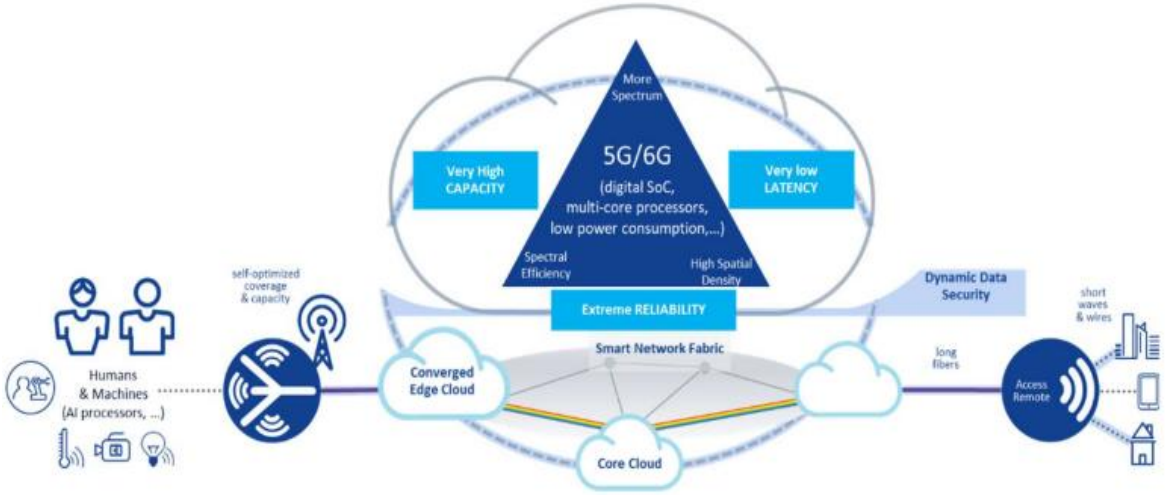


Figure 33. End-to-End System View (Source COREnect project)

An end-to-end view of future connectivity systems is depicted in Figure 33. To meet the needs of emerging applications such as industrial automation, future connectivity systems need to offer extremely high capacity, extreme coverage, extremely low latency and high reliability, all at low energy and low cost. In the global competition, we must consider that China is well ahead of US and Europe in 5G deployment and plans to implement 6G starting in 2029.

Europe will need to strengthen its position in 5G and beyond, e.g. for industrial applications, and become a leader in 6G influencing standards, favouring domestic IP, and capturing future business opportunities. A European ecosystem approach could be developed with intense cooperation between key actors of the semiconductor value chain and the end-users of the equipment industry. European companies can leverage on key strengths in areas such as analogue and RF (radio-frequency) modules, RF-SOI and BiCMOS for high frequency modules, Gallium Nitride and Gallium Arsenide components, low-power embedded computing, power management, silicon photonics, R&D competence in various areas, including heterogeneous integration etc. On the other side there are weaknesses that need to be addressed: digital and baseband processing, manufacturing of leading-edge nodes, industrialisation of II-V materials, industrialisation of advanced packaging, insufficient presence of fabless design, software, IP and EDA companies.

[17] The metaverse, explained: what it is, and why tech companies love it - Polygon

The expected rapid uptake of 5G and 6G will drive the need for III-V materials, heterogeneous integration of chiplets, edge processing. An ecosystem approach, involving key actors of the EU telecom and semiconductor industries, is needed in the near term to capture opportunities in 6G.

4.5 Aerospace, Defence and Security

Semiconductors for aerospace and defence are subject to demanding requirements in terms of performance, reliability and robustness in harsh environmental conditions. Space semiconductors must resist high levels of mechanical and electrical stress during the launch (vibration, shocks) and during operations in the space (radiation, solar wind, temperature variations). In the defence sector, security is considered more important than the use of last generation products. However, new defence programmes will require more and more the access to chips manufactured on leading-edge nodes.

The importance of security of information in space and defence, but also in critical civilian applications (e.g. end-to-end secured communication), requires the development of 'trusted chips'. This implies the certification and qualification of components suited for space, defence and security applications. Driven by space missions in telecommunication, navigation and Earth observation make use of high-performance semiconductors and, therefore, require access to the most advanced technology nodes. This includes semiconductor technologies based on Silicon, but also advanced technologies making use of compound semiconductors (SiC, GaN, SiGe,…) for the implementation of critical system functions together with dedicated packaging approaches (e.g. radiation hard).

Europe's share of electronics for these markets is (22%) compared with China (24%) and North America (19%). The semiconductor market in the military and aerospace industry is estimated in USD 6.3 billion in 2020 and expected to grow by USD 3.89 billion by 2025[18], driven by factors such as increased upgrading and modernisation of aircraft. This is mainly in cockpit electronics as older systems become obsolete.

4.6 Energy

In the energy sector, the efficient production and transmission of electrical power is key to reaching the Green Deal objectives. Europe has particular strengths in this field. On the generation side, Renewable Energy Sources (RES) (such as wind, photovoltaic, etc.) are being deployed to gradually phase out fossil fuel generation. This renewable energy generation needs to be first adapted (inverted, converted) before being connected to the Alternating Current (AC) system. Contextually, Direct Current Technologies (DCT) are being demonstrated as an efficient way to transmit and distribute electrical power in complementarity with the actual AC system. Furthermore, in congested AC grids due to high RES penetration, ad-hoc equipment (STATCOM, FACTS, etc.) are appropriately placed in the grid to control and optimise energy flows.

In all the above applications, power electronics are the key elements for generation, transmission and control of energy by means of inverters, converters and other power conversion equipment and their effectiveness crucially depends on innovative power semiconductors. They represent the key enabling technology for an innovative and very efficient class of power devices suitable for a wide range of power conversion applications, in particular within the High Voltage / High Power types of devices.

[18] Semiconductor Market Scope in Military and Aerospace Industry. Technavio (Dec. 2021)

New production processes with wide bandgap materials (SiC and GaN) significantly improve switching efficiency, and enable higher voltages, higher temperatures and size reduction. The Offshore Renewable Energy Strategy (60 GW of offshore wind and at least 1 GW of ocean energy by 2030, with a view to reach by 2050 300 GW and 40 GW) will lead to an increased demand for inverters and converters with improved efficiencies and capabilities. The forthcoming EU Solar Strategy stresses, amongst others, the need to accelerate the deployment of Photovoltaic (PV) energy. The grid infrastructure which will dispatch the energy to the consumption centres will grow and evolve to an AC/DC hybrid grid to face the challenges posed by the increasing RES penetration. All this will entail an increase in the number of inverters and converters deployed within the grid, with a massive use of Power Electronics.

5. Technology Drivers and Opportunities for the Future

5.1 Edge Computing

Today, 80% of data is processed in the cloud and this market is characterised by few US companies that currently take 80% of the revenue. However, the trend is that the need for computing power at the edge (close to or on the device where data is captured or generated) is growing much faster than the demand for processing in the cloud. It is expected that in 5 years 80% of data processing will take place at the edge reversing today's balance. This represents a huge opportunity for Europe to gain a strong foothold and be at the forefront of leadership in this market.

Already there is a proliferation of so-called edge devices, e.g., smart watches, smart meters, robots, sensors and there are many potential applications, e.g., monitoring the elderly in their homes, optimisation of renewal energy sources, tracking and optimising resource use in factories, optimising pesticide and water use by farm machinery, etc. In all cases, data is collected and analysed locally, close to the device or person in question. By keeping data local, edge computing provides benefits in terms of privacy and reduces energy consumption as less data is sent to the cloud for remote processing. Linkages between application domains, e.g., renewables with EV charging, are also possible to provide further optimisation and generate new business cases.

Edge devices will get smarter and smarter as increasingly higher levels of computational power can be embedded in a device. This will result in a paradigm shift and already there are examples such as autonomous driving happening today with the trialling of ad hoc 5G networks along major highway corridors[19]. In February 2020 the European Commission adopted the Data Strategy[20] and new legislation has been proposed[21]. This naturally puts emphasis on sensors, peripheral equipment and computers used in sectors such as transport, logistics, agriculture, etc.

It is clear that Europe has strengths in systems design for key industrial sectors such as manufacturing, automotive, etc. The key differentiator in future will be in providing trusted hardware/software platforms that can support the non-functional requirements of the application domains. This is an area where Europe is a leader.

5.2 Artificial Intelligence

The advent of AI has been a major disruptive element for the semiconductors industry and it will be one of the main drivers for growth until 2030. This is being driven by the use of AI in data centres, but also increasingly at the edge, e.g. autonomous cars. Beside the semiconductors market leaders such as Nvidia, Intel and Qualcomm, most technology companies such as Google, Amazon, Facebook, Tesla, Huawei, Baidu, have undertaken internal development of AI chips. New players are challenging the incumbents and important investments are being made by venture capital firms in AI chip companies in the US and China. The segment represented by chipsets for AI applications is by far the fastest growing in microelectronics, with expected annual growth rates above 40% for the coming years.[31] Deloitte analysts say AI will become the "next kind of superpower" for nations to compete over, and

[19] Cross-border corridors | Shaping Europe's digital future (europa.eu)
[20] Strategy for Data | Shaping Europe's digital future (europa.eu)
[21] Commission's Proposal for a Regulation on European data governance (Data Governance Act, COM/2020/767 final); Proposal for a Regulation on harmonised rules on fair access to and use of data (Data Act, COM/2022/68 final).

AI chips are the engine to run it. At the same time, however, deep learning models are increasing in size and complexity, requiring ever more computing power.

The quest for AI started in the 1950's, but despite advances in the following decades, computing power remained insufficient until a breakthrough appeared in 2012, when accelerators started being used for deep learning instead of CPUs. The **massive parallelization** of thousands of accelerator cores (instead of typically 4 for CPUs) suddenly provided 100 times higher computing performance, resulting in lower error rates.

Accelerators are capable of performing specific operations at a much higher speed than general-purpose processors. The most well-known type of accelerator is a GPU (Graphics Processing Unit), which is generally employed for rendering real-time high-resolution graphics, but now also applied to high-level parallel data processing. Beside GPUs, there is a wide variety of new dedicated architectures (ASICs) for machine and deep learning accelerators (e.g. Google's TPU: Tensor Processing Unit) which keeps expanding at a fast pace (to train neural networks). For inference (the deployment of a neural network), often programmable arrays (FPGAs) are used. Over the past few years, many new hardware solutions have emerged from both start-ups and established chip vendors optimised for deep learning, natural language processing, and other AI workloads. AI accelerators are entering in all types of computing systems from cloud to edge, from low-power devices to HPC servers.

A fundamental issue is that AI is highly demanding in terms of energy. A machine-learning task can require the power of thousands of computers equivalent to the energy produced in one hour by three nuclear plants. As AI penetrates more of our daily life, such **energy needs are not sustainable**; dedicated electronic components can be much more efficient. It is therefore necessary to share intelligence features between hardware and software. In edge AI applications, considering the massive surge of connected devices at the point of use, maximum power efficiency is essential and many AI functions have to be implemented in hardware.

For its AI needs, currently Europe depends fully on electronic components from non-EU suppliers. Industry leaders (such as Intel, Nvidia, Google, Qualcomm, Huawei) are heavily investing in pushing the limits of parallelization and reduced precision. China has a range of initiatives related to AI hardware promoting its early adoption in industry and society. In addition, the end of Moore's law (linear scaling) in semiconductors opens the way to the rise of new processing solutions and technologies (beyond Moore). Specialized accelerators based on innovative approaches are the future of computing in any type of applications from cloud to Edge AI.

Europe has strong R&D competences in novel semiconductor technologies, such as new types of non-volatile memories for In-Memory and Analogue Computing, Neuromorphic Computing, silicon photonics, and more. Europe is also home to a suitable substrate for mixing analogue and digital processing (FDSOI), a clear advantage for the integration in ultra-low power devices for edge AI. This represents an opportunity for Europe in key digital technologies: by investing in research and innovation in these fields, Europe could gain a leading position in this market, with trusted components that respect core European values in terms of privacy, security, AI explainability and environmental sustainability.

5.3 Increasing Security and Confidentiality Requirements

As the world has become more digitalised and interconnected, security has become a key requirement for electronic devices from the point of view of safety, but also from the point of view of confidentiality.

Security has become a major topic across many sectors including automotive, industrial automation, communications, healthcare, aerospace and defence. For industries such as automotive or healthcare, a security breach can lead to physical injury and/or loss of customer confidence, introducing concerns over liability.

With the introduction of GDPR[22] in Europe personal data needs to be carefully processed. With home working, people are using their own devices which may pose multiple cybersecurity challenges. Devices which are used for both business and personal use may run outdated or pirated software that hackers can exploit to access confidential and valuable business data. It is also easier to gain access to a private network. The average cost of a data breach has increased from USD 3.86 million to USD 4.24 million during 2021[23], due to people working from home. Fewer than 3% of organisations protect their employees' mobile devices.

Figure 34. ST54J Secure Chip Using SoC for Mobile Devices (Source: STMicroelectronics)

Cybersecurity challenges come in many forms, including ransomware, phishing attacks, malware attacks, etc. Ransomware attacks target desktops, laptops, mobile phones and smart security devices. The aim is to compromise sensitive user data in the device itself or render it unusable, or alternatively use it as gateway to other devices for other malicious attacks. As cloud services are being increasingly used for personal and professional data, they are subject to increasing attacks. In phishing attacks, user data, such as login credentials and credit card numbers, is stolen. Here the aim is not to block access but to exploit access.

At the chip level there are concerns about third-party IP or unknowns in the global supply chain that may lead to "backdoors" in devices. General approaches currently used to boot securely and to authenticate firmware are not sufficient when considering electronics deployed in cars, robots, drones, servers and medical devices. There is a need for designed-in robust hardware security (see Figure 34) considering different threats.

Designing active security into a device will impact complexity and power consumption - an issue for battery powered devices. The added complexity may also add other vulnerabilities. With complex designs making their way into automotive, medical and industrial applications, where they are expected to be used for up to 25 years, security needs to be well architected and flexible enough to respond to future security holes and more sophisticated attack vectors. **There is a need to continually innovate to guard against future new attacks.**

Designing to reduce the risk of potential hardware breaches requires a solid understanding of a chip's architecture. This includes partitioning and prioritisation of data movement and data storage, as well as

[22] General Data Protection Regulation (GDPR) – Official Legal Text (gdpr-info.eu)
[23] Alarming cyber security facts to know for 2021 and beyond - CyberTalk

obfuscation techniques and activity monitoring. As chipmakers utilise more customisation and heterogeneity, this is becoming more difficult. The drive for scaling is also driving architects to package components together. This presents challenges as not all components may be inherently secure and many customised accelerators and IP blocks are provided as black boxes.

There is thus a need for ensuring that solutions can be fully audited and checked/verified (e.g. possibility to look for back doors in open source IPs). Notably this is not possible for IPs licensed from 3rd parties. Common Criteria security certifications for simple hardware IP such as smart cards[24] exist, however, for more complex processors, security is still in its infancy and it is not possible to buy a Common Criteria certified general purpose multicore processor.

To get around this companies have to make liability limiting statements based on the hardware's documented interface. However, this may be insufficient as highlighted by **the Spectre/Meltdown vulnerabilities which appeared in 2018 which were unexpected for almost all OS vendors.**

EU Member States agreed to "work towards common standards and, where appropriate, certification for trusted electronics, as well as common requirements for procurement of secure chips and embedded systems in applications that rely on or make extensive use of chip technology."[25] **Reference certification procedures for specific critical sectors and technologies with potential high social impact are necessary**[26]. Certification of these chips for trust and security should cover the value chain up to integration in end products and should be reflected in public procurement and promoted in international standardisation activities.

5.4 Environmental Sustainability

The increasing digitalisation of industry can help in saving energy and reducing deployment of resources. For example, the concept of using digital twins in industrial production allows to reduce power consumption and to minimize production of scrap as results can be better anticipated. In electricity grids, the massive deployment of smart meters and IT-based balancing of decentralised supply and demand helps to make large savings. Semiconductor devices are at the basis of these IT systems, and much more will be needed in the future.

As digital systems are increasingly deployed in sectors where they were not common before, such as construction or retail, the power consumption of IT itself is increasing. Today, the Information and Communications Technology (ICT) sector is responsible for 5-9% of the world's total electricity use and more than 2% of GHG emissions. The demand for semiconductor technologies is expected to double over the next decade and will bring energy and resource savings in the applications it controls. It is essential that newer approaches and technologies which are targeted in the proposed Chips Act must be ever more efficient to reach lower overall energy consumption and reduce its impact on the environment.

As we will point out in section 6.1, new generations of microprocessor chips in general consume 30% less power compared to the preceding one. Concretely, Europe is the leader in the Fully Depleted Silicon on Insulator (FDSOI) chip architecture that has major benefits for advanced and future technology

[24] https://www.sogis.eu/documents/cc/domains/sc/JIL-Composite-product-evaluation-for-Smart-Cards-and-similar-devices-v1.5.1.pdf

[25] Joint declaration on processors and semiconductor technologies | Shaping Europe's digital future (europa.eu).

[26] Regulation (EU) 2019/881 of the European Parliament and of the Council of 17 April 2019 on ENISA (the European Union Agency for Cybersecurity) and on information and communications technology cybersecurity certification and repealing Regulation (EU) No 526/2013 (Cybersecurity Act)

nodes, allowing faster switching speeds, reduced power and a simpler manufacturing process. This delivers a greatly improved power/performance/cost trade-off compared to alternatives such as both bulk and FinFET technologies, which has led to its adoption in automotive, smartphones and many other battery-powered devices.

The efficient production and transmission of electrical power is becoming more important. With the green transition, reliance on combustion of fossil fuels (coal, gas, oil etc.) for power generation and heating must go down. This is only possible with the increased use of alternative power sources for electricity generation (photovoltaics, wind turbines) and new uses such as electric cars, heat pumps etc. Power semiconductors and power electronics are indispensable elements to make this happen. The effectiveness of power inverters and converters crucially depends on innovative power semiconductors. New production processes with new materials (SiC and Gallium Nitride) promise to significantly improve switching efficiency.

The production of semiconductors is itself a resource-intense process. High cost of resources together with the need to reduce the environmental impact has driven the semiconductor industry for decades already to consider the total life cycle of chips. Usage of energy, water, raw materials and release of fluorinated greenhouse gases during semiconductor manufacturing are key concerns, and so sophisticated methods have been developed to work in closed cycles as far as possible.

The environmental impacts of semiconductor production in the EU are regulated, inter alia, by Regulation (EU) No 517/2014 on fluorinated greenhouse gases (F-gases). F-gases are human-made chemicals that are very strong greenhouse gases (GHG), often several thousand times stronger than carbon dioxide (CO2). Under the F-gas Regulation, the semiconductor industry sector is covered by a prohibition to intentionally emit F-gases as well as requirements to take technically and economically feasible measures to minimise unintentional ("leakage") of these gases. In its review of the F-gas Regulation (COM(2022) 150 final) the Commission proposes to reinforce provisions on unintended leakage and require also that emissions must be prevented for nitrogen trifluoride (NF3), a compound also used in the semiconductor manufacturing process.

While the production of semiconductors uses some of the F-gases with the highest global warming potential (e.g. trifluoromethane (HFC-23), perfuorocarbons (PFCs), nitrogen trifluoride (NF3), sulphur hexafluoride (SF6) etc.), the quantities are modest amounting to about a few percent of total current F-gas emissions in the EU[27].

Generally, the EU semiconductor industry is taking stricter measures during its manufacturing processes to prevent emitting F-gases compared to other world regions. The sector is claiming to have made substantial investments to implement reduction practices at operations across Europe. The European Semiconductor Industry Association (ESIA) estimated in 2021 that the industry had achieved a 42% absolute emission reduction of PFCs between 2010 and 2020[28]. If looked at from a global perspective, an increased and significant production of semiconductors in the EU while minimising where possible emissions, is likely to save emissions from F-gases at global scale.

[27] See Impact Assessment to: *Regulation (EU) No 517/2014 of the European Parliament and of the Council of 16 April 2014 on fluorinated greenhouse gases and repealing Regulation (EC) No 842/2006 Text with EEA relevance:*
https://ec.europa.eu/clima/document/download/9013881e-8d5d-429e-9112-c908f127c833_en?filename=f-gases_impact_assessment_en.pdf

[28] https://www.electronicspecifier.com/industries/alternative-energy/european-fluorinated-greenhouse-gas-emissions-cut-by-42

The semiconductor chips themselves do not pose a serious waste problem, as they consist mainly of silicon (typically 99,5% and more) which is hermetically sealed in an inert package. Yet this is different for the electronics boards on which the chips are mounted, to power smartphones for example. These generate electronic scrap after their lifetime, with diverse toxic substances such as cadmium, lead, lead oxide, antimony, nickel, beryllium, barium, chromium and mercury, which may pollute rivers, lakes and seas, and release gases into the atmosphere that upset ecosystems. The recycling of these electronics components is important and regulation to deal with it is in place[29]. At the chip level, methods to prolong the life of chips and equipment and to investigate ways to recycle key materials in order to reduce electronics waste should be considered already at the design stage.

[29] Directive on **waste electrical and electronic equipment** EUR-Lex - 02012L0019-20180704 - EN - EUR-Lex (europa.eu)

EUROPEAN
COMMISSION

Brussels, 11.5.2022
SWD(2022) 147 final

PART 3/4

COMMISSION STAFF WORKING DOCUMENT

A Chips Act for Europe

6. Evolution of Technology to Meet the needs in 2030

6.1 Greater Processing Power

The demand for leading edge chips is forecast to grow much faster than trailing edge chips (See Figure 18). In terms of number of transistors per device this is expected to rise from 100 billion transistors today to 1 trillion transistors by 2030.

The explosion in demand for semiconductors is being driven by ubiquitous computing, the shift towards edge computing, pervasive connectivity and AI applications, which are transforming the world. This in turn requires lower latency, higher density, and more power-efficient processor solutions. To achieve this, **significant R&D investments will be required in new transistor designs, EUV tools, advanced packaging and precision manufacturing for the Angstrom Era of semiconductors**. This will have impacts on automotive, healthcare, retail, banking, etc., where digitalisation is driving radical change and disruption. Graphics and gaming, networking and data processing will all need increased performance, better efficiency, and lower power. The world creates nearly 270,000 petabytes (27 x10^{19}) of data every day[1]. **Intel estimates that by 2030 on average, all of us will have 1 petaflop (10^{15} floating-point operations per second) of compute and 1 petabyte of data less than 1 millisecond away**[2]. This demand for more and more computing power will push the industry to maintain the pace of Moore's Law.

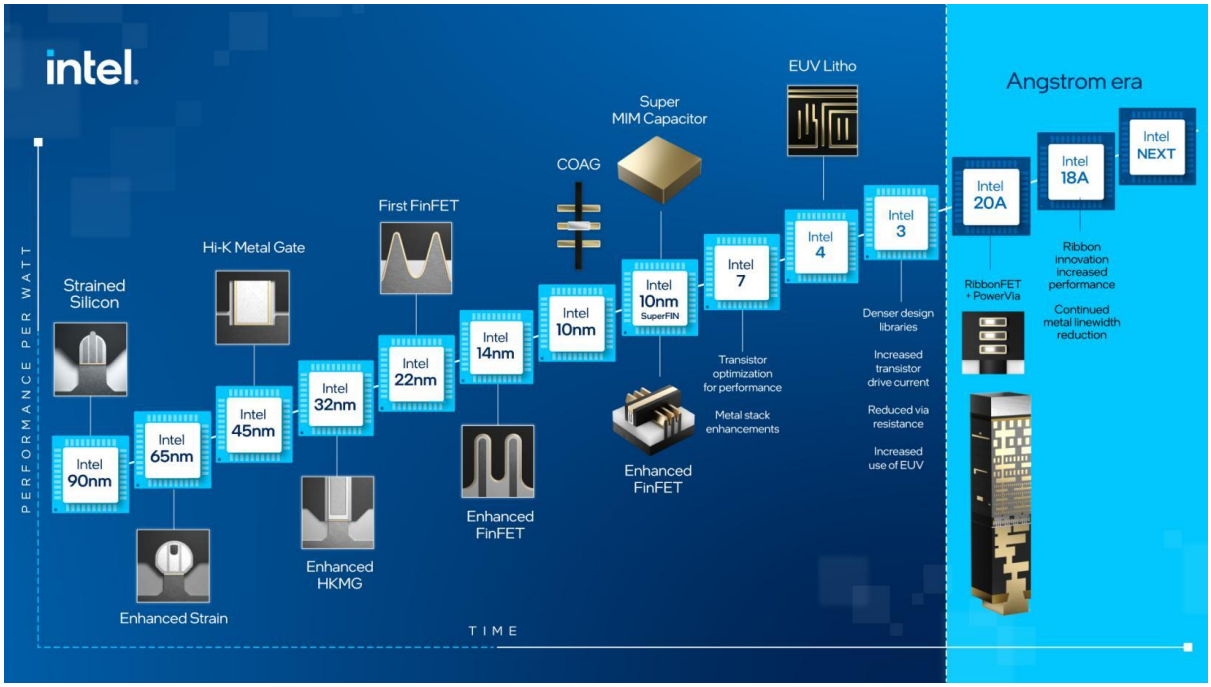


Figure 35. Process Changes and Reductions in Device Feature Size (Source: Intel)

To enable this progress, the industry needs to constantly innovate. As physical dimensions continue to shrink, advances are needed in materials science, new process architectures and design technology co-optimization. For manufacturing, EUV lithography from ASML is being used to improve resolution

[1] According to IDC, 267,906 Petabytes of data are generated every day
[2] Moore's Law - Now and in the Future © Intel corporation

and reduce errors. However, innovation is continuous and new processor nodes are under development to deliver additional gains in power, performance and density.

Successive generations of smartphones, servers and PCs will require ever-increasing computational throughput that can only be achieved at smaller node dimensions. When moving from one semiconductor manufacturing generation to the next there is a 10-15% gain in speed, 20-30% gain in energy efficiency and a reduction of silicon area of about 50% (see figure 36).

Technology generation	Speed gain at equal power	Energy efficiency gain at same speed	Gain in packing density (transistors/mm²)
5nm vs 7nm	15%	30%	x1.8
3nm vs 5nm	10-15%	25-30%	x1.7

Figure 36. Evolution of technology generations for semiconductor manufacturing (Source: TSMC)

Many industrial sectors, such as automotive, industrial automation, healthcare and communications, will make increasing use of AI and edge computing. Such applications will also increasingly drive demand at leading-edge nodes. AI chips require speed and efficiency to cope with vast amounts of data; if deployed at the edge (ie, directly on a device rather than in a remote data centre), better energy efficiency enables them to be integrated into handheld appliances or robots and perform AI tasks locally.

Another key aspect is 3D assembly and packaging. Up until the 2010s, these were used primarily to route power and signalling between the motherboard and silicon, and to protect the silicon. There have been several evolutions (wire bond and lead frame packages, flip chip technology, multi-chip packages), which have increased the number of connections and have allowed Moore's Law further scaling. **Advanced packaging techniques such as 2D and 3D stacking will allow even more transistors per device**. Embedded multi-die interconnect bridge (EMIB) technology allows the use of silicon from different process nodes in the same package, allowing a designer to choose the best process node for that specific IP.

Through the combination of new device technologies, advanced UV lithography and 2.5D-3D packaging, **it is expected that packages with up to 1 Trillion transistors will be possible by 2030.**

Continuous innovation is needed in transistor design, process technologies, lithography and 2.5D-3D packaging to meet the application needs of future devices.

6.2 Device Architectures Tailored for AI

Semiconductors designed to perform AI tasks - AI Chips - are expected to constitute an important market in coming years and companies are **developing specific architectures optimised for AI tasks**. These include AI accelerators and architectures that improve data performance in and out of memory.

Machine Learning algorithms use large data sets to learn and improve. Deep Learning approaches require less data pre-processing by humans. In this area, specialised devices are being developed that allow transfer of large data sets through memory and storage.

Currently, central processing units (CPUs) and accelerators, e.g. graphics-processing units (GPUs), field programmable gate arrays (FPGAs), and application-specific integrated circuits (ASICs) can be used, each with different characteristics and efficiency for different use-cases (see 5.2).

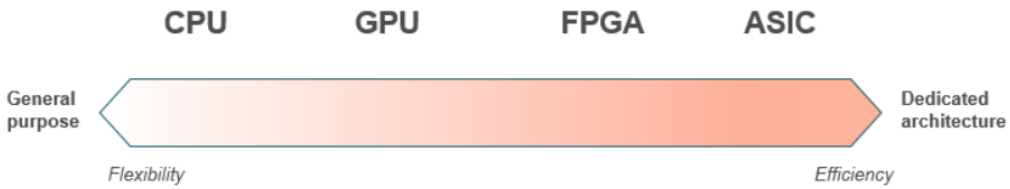


Figure 37. Different types of chips for AI applications

A key need for AI applications **is high bandwidth memory** as the computing layers within deep neural networks must pass input data to thousands of cores as quickly as possible. High bandwidth memory is needed to store input data, weigh model parameters, and perform other functions during both inference and training. This is driving the development of 3D stack of memory that allows Deep Learning to get very fast access to high bandwidth memory.

According to Prof. John Hennessy (Turing Award, chair of Alphabet Inc.), in order to compensate for the slowdown of Moore's Law, **the trend in semiconductors is moving from general-purpose to Domain-Specific Architecture**s: "*the next decade will see a Cambrian explosion of novel architectures, with rapid improvements in terms of performance, as well as in cost, energy and security*". Research is being undertaken in the field. We could group research efforts in microelectronics technologies for AI in the following categories:

- **Massive parallelization** in digital designs: to accelerate matrix operations of deep neural networks;
- **Reduced-precision** acceleration: to speed up computation for deep neural networks, just preserving the needed accuracy;
- **Heterogeneous integration:** Transferring data is a limitation to speed and is power-hungry. Near-memory computing aims at bringing data and processing physically closer; one solution is stacking memory and logic with 3D integration.
- **In-memory computing** performing compute functions in memory to gain speed and power efficiency.
- **Analogue AI** devices: Analogue computing can lead to more "explainable AI" than digital systems mostly operating as black boxes. It can be faster, much more energy-efficient and more "explainable" than digital approaches.
- **Neuromorphic computing** is also called "brain-inspired" computing as it mimics neuro-biological architectures. Its implementation with analogue and in-memory computing can lead to high energy efficiency (100 to 1000 times), making it extremely suitable for Edge AI applications.
- **Photonics AI** is a new research field that aims to mix electronics with optical elements to decrease power and latency in deep neural networks. Silicon photonic chips can exploit optical propagation, and their integration in image sensing devices can lead to ground-breaking efficiency.

New domain-specific architectures, including ASICs and novel semiconductor technologies, will be driving the implementation of neural networks in the booming market of AI chips.

6.3 Open-Source Hardware - RISC-V

The increasing adoption of open source is disruptive as it drastically lowers the barrier to design. China, the US and India, among others, are already investing heavily in open source hardware and software and in order to develop a competitive advantage in key sectors, Europe should support the development of a collaborative ecosystem in this field. The open-source hardware ecosystem is wide ranging and

diverse including the semiconductor industry, verticals and system integrators, SMEs, service providers, design tools providers, open-source communities, academics and research.

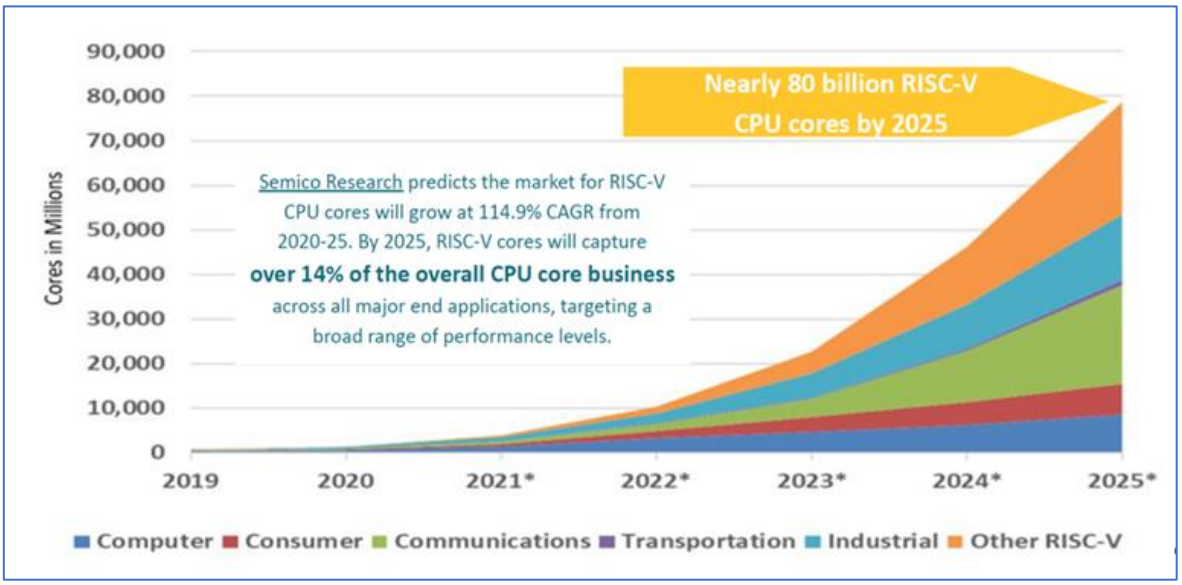


Figure 38. Predicted Growth in RISC-V Market[3]

The predicted growth in the open-source RISC-V[4] CPU market is shown in Figure 38. The benefits and attraction of adoption of open source depends on the type of actor and their role within the value chain. These can include:

- Creating innovative products with lower costs and access barriers.
- Providing a faster path to innovation and smoother cooperation between actors (academic, research, industry, SME, alliances) as no Non-Disclosure Agreement (NDA) and commercial license need to be negotiated.
- Influencing technical choices and specifications.
- Allowing customization of open-source IP to user needs, delivering differentiating products.
- Sharing development costs.
- Reducing risks related to third-party IP (unbalanced commercial relationship, end of maintenance/ discontinued products, export control and trade wars).
- Building support and design service businesses based on open-source IP (such as RedHat).
- Better auditing of security and safety, ensuring that solutions can be fully audited and checked/verified (e.g. possibility to look for back doors in open source IPs). This is not possible for IPs licensed from 3rd parties.

Key areas of interest in the domain are the development of RISC-V compliant processors and accelerators targeting machine learning and cryptography, as well as high-performance storage and communications applications. The use of extended instruction sets to enable more parallel processing, such as RISC-V "P" for Single Input Multiple Data (SIMD) processing and RISC-V "V" for full-scale vector processing, can provide significant performance and/or efficiency gains. However, even higher gains are achievable in many cases by adding application domain-specific features to a hardware architecture.

[3] Semico Research Corp., March 2021
[4] RISC-V is an open standard instruction set architecture (ISA) for microprocessors, based on established reduced instruction set computer (RISC) principles, which is provided under "open-source" license (no use fees).

6.4 EDA Tools and Ecosystem

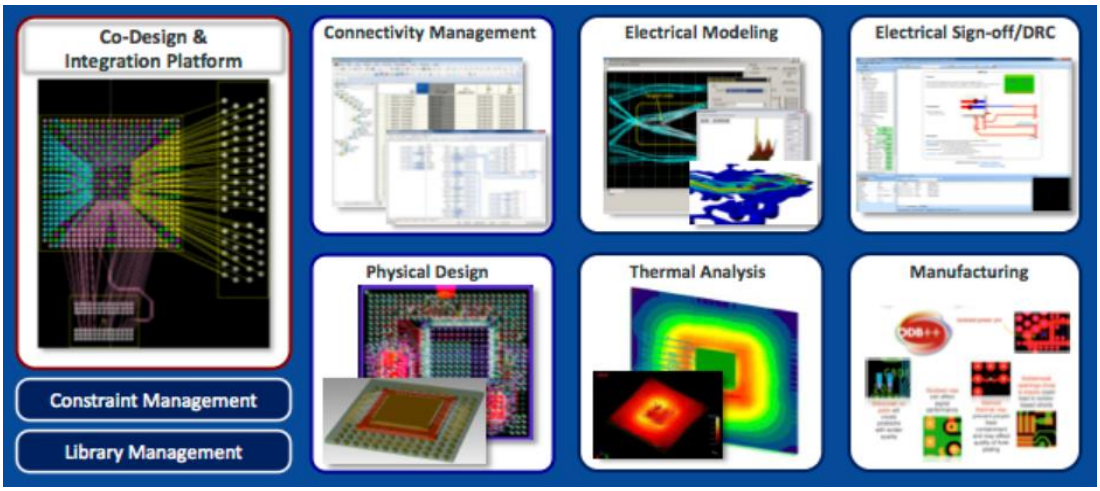


Figure 39. Xpedition Package Integrator Suite (Source: Siemens)

Chip designs can contain tens of millions of logic gates (standard cells) and thousands of memory blocks (macroblocks) made up from billions of transistors, all carefully placed and interconnected by several kilometres of wiring. The placement of these cells and blocks on the chip is critical to the functionality, speed, power consumed and cost of the chip. Electronic Design Automation (EDA) is thus essential for chip design helping designers simulate functionality, integrate IP, optimise floorplan and verify designs. Foundries are also dependent on EDA tools, particularly when presenting coded versions of their manufacturing processes (design rules checks) to design houses to ensure manufacturable chip layouts and reduction of prototyping cycles in design-technology co-optimization. Given the increasingly complex chip design requirements for high performance computing, 5G, AI/ML, IoT, and edge computing capabilities, EDA companies have been prolific acquirers of smaller IP houses to provide integrated, synergistic IP solutions along with their EDA software, becoming significant semiconductor IP houses in their own right. Examples of this are Cadence, Synopsys and Mentor Graphics. A challenge is that the US controls 70% of the global market for EDA tools. However, with the acquisition of Mentor Graphics, Siemens has now become a major player. This offers the opportunity to link and join forces with the European EDA community to collaborate on activities to support European growth in a sector where Europe has very poor presence[5]. The top EDA companies spend more than US$ 1billion annually on R&D costs to continue innovating, so to provide meaningful progress continued investment from the public sector and cross-border collaboration are needed.

As the commercial vendors mostly provide closed source tools, there a move can be observed towards open source tools to support specific parts of the design flow. **Open source tools are essential for introducing new companies and more developers into the field, especially developers with a software background who can bring in innovation in hardware-software co-design**. Developers can freely work together across teams and organizations using massive collaboration hubs such as GitHub or GitLab.

Smaller companies and research organizations need access to professional EDA tools which the large EDA vendors provide through a variety of business models (Cloud offering, specific terms for start-up,

[5] European chipmakers using US-origin IP have to apply for licences to export to China. See chapter 3

research licenses, Software as a Service (SaaS), etc.). The European Commission has proposed to invest in a European open source EDA tooling ecosystem, encouraging open interchange formats and making sure current tools do not introduce restrictions on utilization of open source hardware designs. EDA tools can be exploited in various parts of the development chain including lifecycle management, architecture exploration, design and implementation as well as verification and validation. A key area for the future is in creating transparent, auditable processes for ensuring safety.

By focusing EU investment on tool development and interoperability standards, a mixture of open and closed ASIC tools can be used by designers for future designs supporting RISC-V and chiplet development.

6.5 More than Moore

Moore's Law[6] has driven mainstream microelectronics for several decades resulting in ICs with transistor dimensions at 45 nm and below. While this supports memories and microprocessors, interfacing with the analogue physical world does not scale in the same way. **Radio frequency (RF) devices, power management subsystems, passive components, biochips, sensors, actuators, LEDs, lasers, photonic integrated circuits, microelectromechanical systems (MEMS[7]) now also play an important role in today's semiconductor products.** There is thus a need to integrate analogue functions into CMOS technologies to add value. These devices are called "More than Moore" devices.

The main technical challenges with More Than Moore devices is that they may require unique structures and different materials to those traditionally used. In many cases devices can be fabricated using tools and processes originally developed for older, larger nodes. However, enhancements may be needed with new processes and materials to be deposited and etched. One key challenge is the need for tighter dimensional control. Notably analogue circuits do not benefit from small geometries. Slight variations in one component can have unexpected consequences throughout the circuit which makes them very challenging to design and produce. Providing and managing power is an essential requirement for every device. To do this, some devices are designed with thin vertical structures with large lateral dimensions and some exploit wide band-gap semiconductors like gallium nitride and silicon carbide. There is a need for advanced design technologies to address the challenges of modelling and simulation of reliability, degradation effects and process variability. There is also a need to develop smart fabrication, fab automation and data processing to generate a smart infrastructure. Wafer bonding is a key enabling process technology. There are many applications in low-power devices including energy harvesting, low-power energy conversion and management.

The long-term progression of Moore's Law requires overcoming the exponential growth in the power consumption requirements of current CMOS-based computing[7]. To continue this and create ultra-low power solutions, it is necessary to exploit the quantum effects in materials. This needs to be achieved at ambient room temperatures.

6.6 Quantum Technologies

Quantum Technology (QT) is set to have a substantial impact on the European Union's core industries, including pharmaceuticals, chemicals, and automotive (see Figure 40). **The total combined market**

[6] The number of transistors on a chip doubles every 18 to 24 months
[7] https://www.businesswire.com/news/home/20180809005360/en/

for QT at the end of 2021 is EUR 1.7 billion. This is expected to rise to EUR 10 billion in a technologically conservative scenario, and to EUR 89 billion by 2040 in an aggressive disruption scenario.[8] Overall the effect of QT on the entire economy will be very significant. It could, for instance, transform the ways we develop new drugs, perform medical imaging exams, find optimal portfolios, discover new materials, or the way we communicate securely. These technologies could disrupt the business models of leading players today, giving rise to a range of new products and business models.

Quantum chips are devices that process quantum information, that is, information at the level of individual quantum systems. The level of integration of components onto a single chip varies depending on the technology used. These quantum chips can be used for different applications across the four Quantum Technology pillars that are quantum computing, quantum simulation, quantum communication and quantum sensing and metrology. Standard chips are mainly used in computing machines, but their number is steadily increasing in networks for communication purposes. Similarly, quantum chips are used in computing machines (either as stand-alone quantum computers or accelerators for supercomputers) or in networks where they can provide entirely new services like ultra-secure communications or ultra-precise time. Advances at PASQAL[9], Alpine Quantum Technologies[10], Alice&Bob[11] or IQM[12] , indicate that quantum machines with incredible power are becoming within reach and could be used for rewriting encryptions or accelerating research in numerous industries, including the pharmaceutical industry, material science, logistics, and finance. Such quantum machines are going to be deployed in the market soon and the quantum advantage demonstrated by some of them will soon translate into an industrial advantage as new algorithms are developed and the integration within HPC environment progresses. Quantum chips are also concerned sensors where both low-end (large volumes and cheap) and high-end (low volume and very expensive) quantum sensors need to be pushed toward industrialisation. Quantum communication devices represent another application of quantum chips allowing highly secure communication.

[8] The Rise of Quantum Computing | McKinsey & Company Excludes internal investment by major technology companies such as IBM and Google.

[9] Pasqal Quantum Computers Coming to Azure Quantum (hpcwire.com)

[10] Compact quantum computer for server centers: Researchers build smallest quantum computer yet based on industry standards -- ScienceDaily

[11] Alice&Bob, a quantum computing startup, raises $30M to launch its first fault-tolerant ‘cat qubit’ computers in 2023 | TechCrunch

[12] European quantum computing startup takes its funding to €32M with fresh raise | TechCrunch

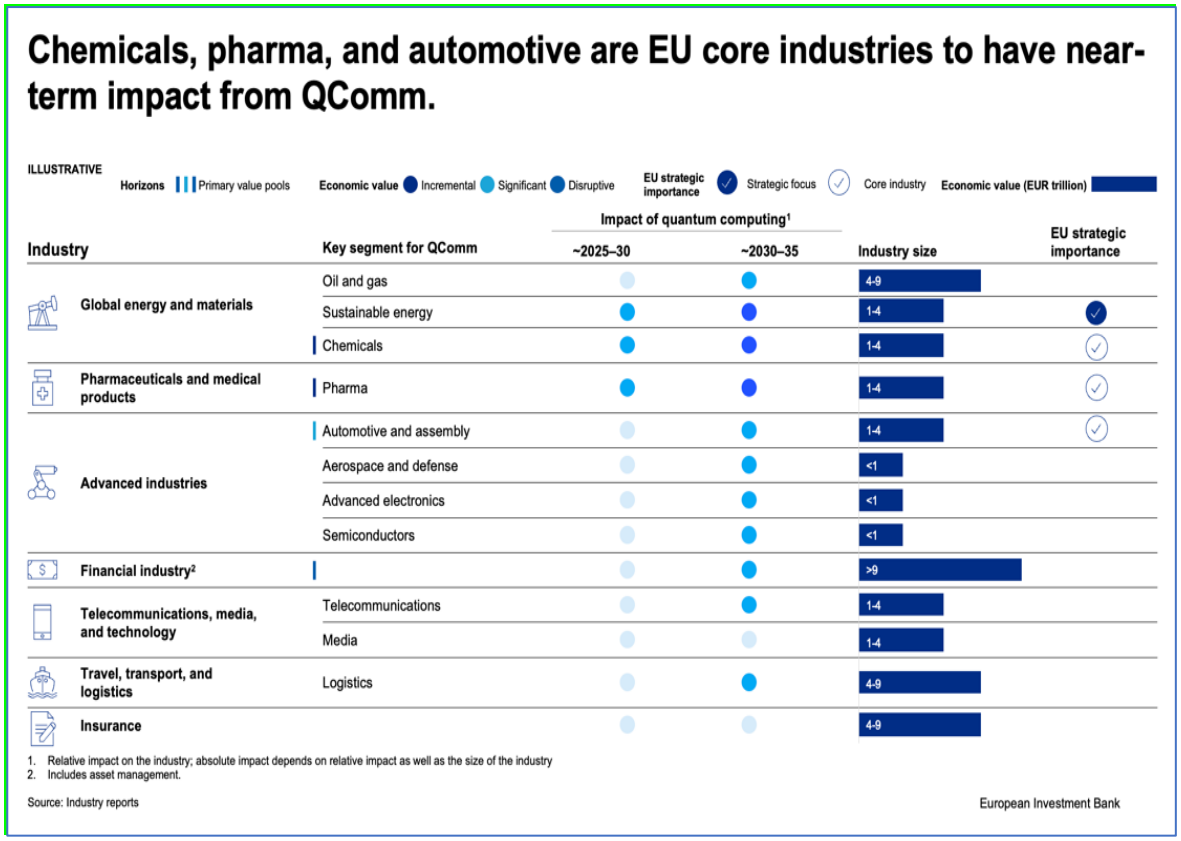


Figure 40. Potential Quantum Technology Markets in EU

In 2018, the European Commission launched the Quantum Flagship, a ten-year initiative with a budget of one billion euros. The European Union, that is, the European Commission and Member States, have also announced EUR 6.1 billion of government funding over the next seven years.[13] The aim is to build on European scientific excellence in quantum and bring research results closer to industrial exploitation and real-life applications, fuelling innovation. Europe has established a climate for QTs that has enabled the number of EU start-ups to grow at a faster rate than in other countries. However, according to a study from the EIB group, these QT start-ups are unable to raise sufficient private Venture Capital funding in Europe[14]: as of the middle of 2021, **around 25 percent of QT companies globally are based in the EU, yet the region has received less than 5 percent of global funding.** Particularly the development of hardware components for QT is capital intensive, and EU deep-tech start-ups in this sector need further dedicated support to attract private investors and bring their innovation to the market.

[13] Some Member States have already established large national quantum programs, notably France (EUR 1.8 billion), Germany (EUR 2 billion) and The Netherlands (EUR 0.65 billion), with complementary objectives and activities such as the knowledge transfer from the research labs to industrialisation, supporting the emergence of a European quantum industry, including design and production capabilities of quantum chips.
[14] "Financing a quantum technologies industry in Europe", McKinsey, EIB, 2022

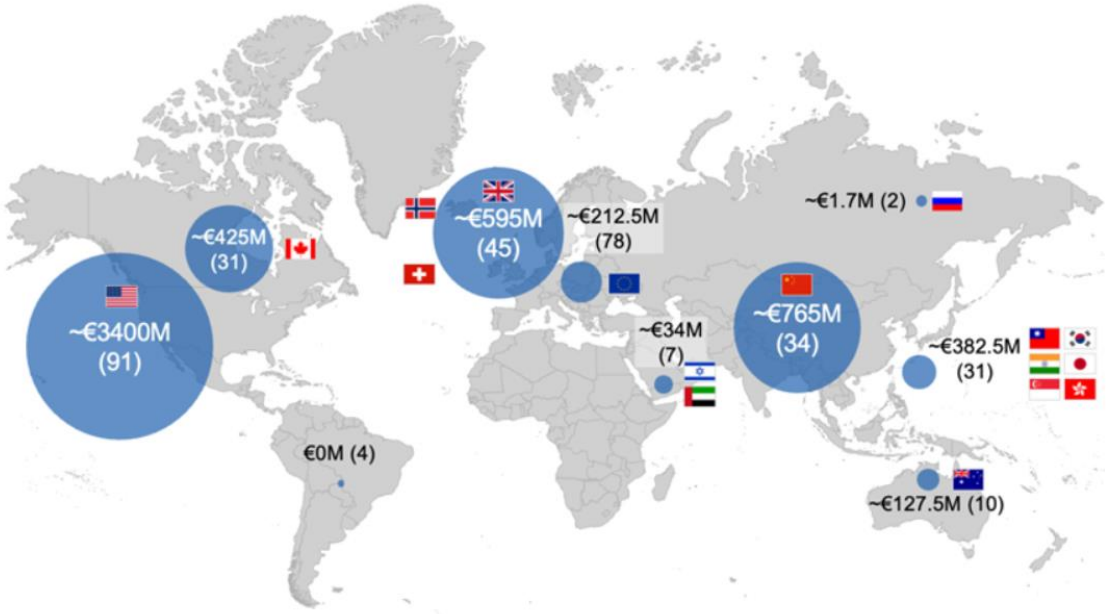


Figure 41. Funding (and number) of QT players by region. Sources: EIB, McKinsey,

The most critical parts are control electronics (possibly cryogenic control electronics), connectivity, and I/O (especially measurements). Despite not being part of quantum chips per se, these components are key to the development of QT (particularly for superconducting and solid-state qubit platforms and single-photon detectors based on superconductors). Importantly, the production of cryogenic control electronics may require specific equipment in the fab facilities. **Quantum chip innovators also need access to dedicated clean rooms and foundries for prototyping and production.** Currently, some European quantum chip innovators are obliged to make use of US facilities, as they do not have access to the relevant facilities in Europe[15].

Europe is a leader in Quantum Technology research. In order to turn research investments into market innovations, quantum devices need to be fabricated. Quantum chips need specialised facilities and if Europe does not invest, key innovations will either fail to reach the market or will go abroad for financing.

[15] Second workshop on Quantum Chip Act organised by the EC with participation of academia, RTOs and Industry representatives, 19 October 2021.

PART II - A Plan for Action

7. The Chips Act: the way forward

As mentioned in **Chapter 1**, the production of chips relies on collaboration and trade between the major semiconductor-producing regions. Complex interdependencies across the value chain and many potential choke points, stemming from concentration of essential technologies or activities within particular companies or geographies (more than 70% of foundry services are in Asia, for example), makes it prone to disruption. As illustrated in Chapter 1, failures or shortages at any point in the value chain can have repercussions across the full supply chain.

These structural weaknesses coupled with lean production strategies and geopolitical tensions, which had interrupted established trade flows even before the pandemic, left the industry unable to cope with the surge in demand following the onset of the pandemic. The impact of the ensuing shortage on the European economy has been severe. As set out in **Chapter 2**, automakers are still having to wait for periods of up to a year or more for chips; many have had to reduce production or shut down, laying off workers.

Many other sectors have been impacted by the shortage, which has brought to light the degree to which semiconductors have penetrated every facet of society. Yet they will continue to find increasing use; the market for semiconductor chips is expected to double between 2020 and 2030 to a value of more than USD 1 trillion.

However, as shown in **Chapter 3**, the level of consumption of semiconductor components in Europe is much higher than (around twice) the value of components produced in the EU or even the value of components produced by European companies globally. In 2021, the EU's trade deficit for semiconductors was almost EUR 20 billion with exports amounting to EUR 31.5 billion while imports amounted to EUR 51 billion. And in 2021, fabs were operating at full capacity.

The EU has observed in the last 20 years a gradually declining share of global manufacturing capacity. Moreover, roughly 50% of capacity in the EU is concentrated at nodes of 180 nm and above. Design competences are largely concentrated on analogue, power, microcontrollers and MEMS - important for systems operating in the real world; for processors and memory components - central to computing - competences are scattered and confined to niche applications. This is reflected in industrial research efforts which have focussed on the former, rather than equipping the Union for digital transition (see also section 3.3.3).

These are major concerns in light of the fact that future market growth is forecast to be concentrated below 10 nm nodes, where chips are needed to process ever-higher volumes of data, perform at higher speed and with less energy consumption. Application domains where the EU needs to maintain and build resilience - automotive, industrial automation, communications, aerospace, defence and security - will on the one hand continue to rely on many types of analogue, power, microcontrollers and MEMS components, and on the other make use of leading-edge processors (10 nm and below) to perform tasks autonomously as presented in **Chapter 4**. Chapter 4 also points to needs in advanced packaging/ heterogeneous integration, wafers and materials for power electronics and communications, and a more assertive approach in standards (healthcare, automotive, communications and security).

By leveraging existing industrial strengths in security and its lead in R&D on new computing paradigms that enhance computational power and drastically reduce energy consumption, the EU has a real opportunity to capture market shares in strategic emerging technologies such as edge-computing and AI. As set out in **Chapter 5**, edge computing and AI will be widely deployed i.a. in automotive and

industrial market segments where the EU's strengths in system design lie; sustainability and security will be key differentiators in these and many other future markets.

However, leading technology companies in other regions are making large investments in squeezing more transistors into ever smaller volumes of silicon, in a race to master next generation technologies such as GAAFET and RibbonFET, and advanced packaging techniques such as 3D stacking and chiplets. These companies are also active in exploring new device architectures for AI and quantum technologies. Europe is at the cutting-edge of R&D in these domains; with the possible exception of ASML however, there are few European industries actively exploiting the fruits of such R&D efforts as shown in **Chapters 3 and 6**.

Open-source approaches and open platforms can reduce dependencies on a limited number of suplliers and European companies are attempting to make strides in design with open hardware platforms to generate IP for accelerators and processors, and open source EDA tools. However more can be done, for example in advanced packaging.

In terms of technology capacity, the EU clearly has strengths that it can build on, but has serious gaps which if not addressed could even lead to current strengths being eroded.

It is against this backdrop that the European Commission presented the Chips Act package, with measures and actions to address the weaknesses outlined above. These weakness can be grouped under the following 3 headings with the three foundational pillars in response - further elaborated in **Chapter 8**:

Limited innovation capacity in the ecosystem

- The EU's research programmes have largely not driven **the conversion of its excellent research results into industrial innovation**. They have fallen short in stimulating the partnerships at industrial (end-user) level that would exploit such developments and in playing a leading role when it comes to driving new trends, platforms and standards.
    - For example, the EU has pure play foundries as well as IDMs with in-house production facilities and some few companies active in back-end manufacturing. While these companies perform well in specific market segments, many of the world-leading innovations developed by the EU's RTOs and are taken up in other parts of the world. Consequently they have not led to diversifying and strengthening the EU's manufacturing base, in particular as regards digital technologies and leading-edge nodes.
    - **Similarly, while the EU has important strengths in systems design, it has significant weaknesses in digital design** and in particular in processors. As explained in section 3.3.3, this can in part be attributed to a focus by companies on core business, even when it comes to investing in R&D. Furthermore, EU systems houses (end-user companies) have been less present in research activities focussed on semiconductors, which limits the diversity of efforts by suppliers and is a missed opportunity to strengthen user-supplier relations which can stimulate transfer of results into innovation.
- **SMEs and start-ups have difficulty attracting the necessary investment** to develop their ideas and scale. This has led to stagnating growth of an indigenous European ecosystem and ultimately

creating gaps at the cutting-edge of technology. Specifically, the EU's footprint in the fast growing fabless design segment has declined to less than 1%[16]. mergr

- **As the EU industry has pointed out in a report published in 2018,[17]** the EU has a limited pool of talent, and lacks a workforce with the necessary skills.

To address the above, **Pillar 1 of the Chips Act, the Chips for Europe Initiative**, will create an ecosystem to build up coordinated R&D efforts and technological capacity at scale throughout the Union. Through the set-up of large scale-pilots and a virtual design platform – that are designed in consultation with industry – to ease and accelerate the testing and validation of new concepts, and their transition to commercially viable products, it will provide conditions for European industry to create and deploy cutting-edge technologies to capitalise on the opportunities ahead in domains such as AI and edge-computing, and supply the needs of key sectors (such as automotive, industrial automation, communications, healthcare). Through a network of competence centres it will facilitate access to these facilities by stakeholders across the Union and will further develop the diverse initiatives on skills. It will also deploy a Chips Fund with the aim of facilitating further growth in particular of smaller innovative companies active in design and integration.

With the exception of the Chips Fund, the above activities will be implemented under the Chips JU which will replace the KDT JU. To assure its strategic alignment with the goal of strengthening Europe's semiconductor ecosystem, the EU and national authorities will outline the work programme – taking into account advice from relevant stakeholders.

Low investment in manufacturing capacity

- The EU depends excessively on production capacities located in third countries - it is a net importer of semiconductors, particularly for the most advanced ones at the leading edge – in fact, it has no foundries for nodes smaller than 22 nm.
- The EU also depends on third countries for certain types of wafers such as SiC and GaN, the availability of which will be crucial for further innovation in the automotive, communications and energy sectors, and for the realisation of EU's green transition (see sections 4.2, 4.4 and 4.6).
- The shortage has served to highlight vulnerabilities throughout the **entire** supply chain. EU-headquartered (and other) companies face difficulties in acquiring microcontrollers, analogue, opto-electronic and other chips including those for which the EU has fabrication facilities and despite their running at full capacity.
- Given the continued increase in demand for semiconductors, companies needing smaller volumes of specialised chips are particularly hit by the crisis, including those who produce equipment needed for chip-manufacturing[18].
- There have been bottlenecks due to packaging being concentrated in South East Asia where problems with transport and logistics continue to persist (see section 2.6). Shortages of materials also slow production and can bring it to a halt.

[16] Sales growth of fabless companies in 2020 is 24%, compared to 8% for IDM companies. Source: IC Insights/McClean report 2021.
[17] Boosting Electronics Value Chains in Europe, June 19, 2018
[18] Chipping In For Equipment Suppliers: The Equipment Multiplier Effect On The Chip Shortage, Semiconductor Engineering, May 2022

- Currently, less than 4% of global CAPEX investments by the sector are made by EU headquartered companies. The ever-increasing costs and complexity of establishing production capacities mean that investments can be highly risky; furthermore there are long lead times before investments translate to increased capacity.

To address the above, **Pillar 2 of the Chips Act, Security of Supply**, proposes to make use of a framework that contributes to the security of supply and that can help to strengthen the resilience of the semiconductor ecosystem in the EU, by fostering investment in first-of-a-kind facilities which should be beneficial for the entire semiconductor ecosystem in Europe. These can, moreover, be expressly mobilized for critical sectors or important economic sectors in Europe in times of crisis.

Imbalance between supply and demand

- Disruptions in the supply of semiconductors have very negative effects on Europe's economy and society. The complexity of the semiconductor supply chain makes it difficult to identify and assess risks related to potential shortages and take the appropriate mitigating action. This will require more transparency together with more detailed information to be provided regularly by industrial stakeholders.
- In response to shortages, some Member States (MS) have announced their intention to take unilateral action to be able to anticipate and mitigate possible disruptions, as cooperation on effective, coherent actions is lacking at EU level.
- There is a lack of a coordination mechanism between MS and the Commission as well as among MS themselves with relation to efforts in the field of semiconductors.
- In the toolbox of the Commission and of the MS, there is a lack of effective instruments that may help addressing potential shortages.

In response, **Pillar 3, Monitoring and Crisis Response**, will establish a coordination mechanism between the Member States and the Commission to better anticipate and mitigate the effects of shortages. It includes a monitoring scheme and a crisis mechanism with a dedicated toolbox of measures that can be triggered in the event of a crisis.

Why this proposed course of Action?

On 23 May 2013, the European Commission announced An Electronics Strategy for Europe[19], with the objective to reverse the declining European share of the world market, and to ensure that Europe makes the best of semiconductor technology to boost innovation, growth and jobs creation across the economy.

Specific targets were, by 2020, to facilitate industry investment of €100 billion; double the value of EU micro-chip production; and create 250 000 jobs in Europe. The strategy was implemented primarily by means of the ECSEL JU and by making use of the IPCEI instrument. The latter was initiated in recognition of the fact that a new qualitative and quantitative approach was needed in order to allow industry to invest again in Europe as is done in the rest of the world. The IPCEI requires innovation to be beyond the global state-of-the-art which limits its utility. Nevertheless both initiatives served to unleash investment in Europe (see section 3.3.3). However, the concrete targets have not been met – in

[19] 'Communication from the Commission to the European Parliament, the Council, the European Economic and Social Committee and the Committee of the Regions — A European Strategy for Micro- and Nanoelectronic Components and Systems' COM(2013) 298 final

particular the EU's share of production is declining as investment in other parts of the world continues to increase. There are several reasons for this, notably:

- The agenda for R&I has been very much industry driven[20] and therefore largely focussed on shorter-term core business interests; policy-makers (the Union and Participating national authorities) did not have the possibility to be proactive in driving investment in longer term strategic targets.
- Despite the emphasis given to the importance of involving demand-side industries, their participation was very limited.
- The EU potential to design chips was given insufficient attention.
- While the sector was confronted by increasing geopolitical tensions - driven inter alia by intense competition between the US and China[21]; technological and economic challenges - as miniaturisation becomes ever more complex and costly; use of subsidies[22] which distorted the playing field; the EU was equipped with limited means to respond.
- The lack of an over-arching framework to monitor progress towards the targets meant there was little drive or impetus at EU level, and limited awareness of the strategic importance of the sector.
- Action around skills and investment funds were part of the 2013 strategy, however microelectronics was bundled with other so-called Key Enabling Technologies, and follow-up specific to the sector was minimal.
- Despite the Union having agreed to an increase in the budget of the KDT JU, relative to its predecessor, for the 2021-28 Multiannual Financial Framework, the lack of shortages did not create the necessary political momentum for policy makers in all countries to embrace the initiative through new instruments.

The shortages of semiconductors have been an instigator of change. It has raised awareness at all levels of society of the critical role of semiconductors for the economy. The Chips Act represents a holistic response to the shortage bringing: increased funding to support research and capacity building and new mechanisms for implementation; a driving role for the Union and Member States – in consultation with industry - for defining areas of strategic interest; more focus on harnessing Europe's chip design capability; dedicated activities on skills and investment funds; new concepts, such as "first-of-a-kind facility in the Union" for establishing security of supply; and mechanisms to define indicators to understand the state of the industry, monitor the supply chain and to mitigate the effects of crisis.

This represents a step change from the past.

Coordination across all three pillars of the Chips Act will be of the utmost importance therefore to ensure coherence, effectiveness and efficiency of implementation. Given the existence of bodies such as the governing boards linked to the current KDT JU and the Alliance on Semiconductors and Processor Technologies, and the need for a coordination mechanism for the implementation of Pillar 3, a clear Governance structure will need to be put in place, to define the roles of and interactions between participatory bodies, and to drive and monitor progress.

[20] Interim evaluation of the ECSEL JU
[21] With the announcement in 2015 by China of its Made in China Initiative
[22] Measuring distortions in international markets: The semiconductor value chain, OECD December 2019

Subsequent to agreement by Member States on the KDT JU, an IPCEI with substantial participation from Member States and industry has been pre-notified to the Commission. This represents a positive EU-wide effort to mobilise resources towards strengthening the European ecosystem.

8. The Three Pillars of the Chips Act Package

8.1 Pillar 1. The Chips for Europe Initiative

8.1.1 Introduction

As discussed above, Europe's research programmes were not designed to bridge the gap to production, and hence have not translated its excellent research results into industrial excellence and market breakthroughs. In contrast, investments in Europe have tended to be focused on particular technologies such as power electronics, RF and analogue for specific applications, but generally not in mainstream digital technologies.

Industry, with support from Member States, has of late begun to step up on investments in both R&D&I and First Industrial Deployment. 19 Member States have recently pre-notified a second[23] Important Project of Common European Interest (IPCEI) to the Commission, with more than 100 industrial participants (up from 32 in the first IPCEI). In terms of technologies and application domains this goes beyond the first IPCEI in putting for example also communications as a major focus; it addresses R&D&I and First Industrial Deployment of a range of advanced microelectronic technologies and supports their application in downstream industries. The proposed IPCEI has mobilised a large number of SMEs from across the Union and has served to raise widespread awareness of the Union's efforts to promote investment in semiconductor technologies.

This is a positive development, but a more coherent response is needed to address the set of problems outlined in Chapter 7 and the preceding chapters above. Europe needs to establish and invest in an infrastructure to develop knowledge and expertise in building technologies such as processors as well as new emerging technologies such as AI, neuromorphic, quantum etc. It also needs new semiconductor production nodes below 10 nm to satisfy upcoming market needs, as explained in Chapters 1-6. Building this expertise and capacity in Europe at an industrial level is essential for Europe to stay at the forefront of innovation; the only way to achieve this is to invest in new infrastructures in design platforms and pilot lines as outlined below.

8.1.2 Explaining further the Pillar 1 approach

The Chips for Europe Initiative (Pillar 1 of the Chips Act package) was designed to address the research, development, and infrastructural gaps in Europe. It aims to invest in activities that would **close the gap from lab to fab**, by

i) **Leveraging European strengths** – starting with existing capacities and research expertise
ii) Further **reinforcing technology capacities** – which implies addressing the gaps and preparing for longer-term capabilities.

That will only work through a **collective effort by all stakeholders**: EU and Member States across the Union; industrial actors across the full value chain; researchers and RTOs. A concerted set of activities would start with **design** that has to date been a weakness in Europe, which is also reflected in the lack of indigenous fabless companies. A good base in design capabilities is needed to feed into the rest of

[23] Details of the first IPCEI are provided in Ch 3.

the innovation value chain and prepare for the necessary components, systems and ultimately products to be developed and produced in Europe.

To this end the **Chips for Europe Initiative** proposed to set up:

- **A (virtual) design platform accessible across the EU** offering Electronic Design Automation (EDA) tools , IP libraries (created and combined by RTOs and participants across the EU) and integrating and standardising libraries from **existing pilot lines** (see Annex 5). The idea is to provide user-friendly routes to design of new functionalities or new chips and systems for innovative SMEs, IDMs, fabless design companies and vertical industries.

- **Pilot lines that are open for research, testing, experimentation and validation** of new device concepts. The idea is to start with existing pilot lines (e.g. from the ECSEL JU) and **bring them to a higher level of maturity** to facilitate research, development, test, experimentation and validation of these novel technologies by industry in their designs. By carrying out research on the pilot lines, the whole innovation cycle will be accelerated.

Europe needs to catch up in its innovation capabilities in design and development as quickly as possible. The best way to achieve this is to develop a design platform that will use the existing capacities and infrastructures in a way that will help industry shorten its design and development cycle. This will be done by creating **a virtual platform**, providing users with Electronic Design Automation (EDA) tools and integrating libraries from **existing pilot lines** (see Annex 5) that can be used for designing new functionalities or new chips and systems. This would all be networked together and made widely available in Europe, creating a large capability with potential innovations in all relevant technologies such as FDSOI, FinFET, heterogeneous integration, and silicon photonics, but also others for particular applications. Starting in this way with existing pilot lines now will enable production in the respective technologies in **2024-2026**. At the same time, it is essential to set up **new pilot lines** to create capacities where the EU has gaps, notably in design and production at advanced nodes, by **2027-28 and beyond**.

8.1.3 Investing in a pan European virtual design platform

The design platform will be **available to users across Europe**. It will be continuously upgraded with new design capabilities. In this way it will stimulate a wide cooperation of users' communities with design houses, IP and tool suppliers, designers and RTOs, and cater for the design of novel components and systems for multiple applications such as low energy, security, system integration and 3D assembly. To exploit synergies across pilot lines, design elements specific to each pilot line will be integrated in a broader design environment providing designers with a common structure that is more efficient and richer in technology options.

The **design platform** will also provide for creation of **virtual prototypes** based on technology that does not yet exist physically. This would in turn allow different integration technologies and manufacturing options to be explored. Such early insight will boost the European design ecosystem for the advanced nodes, allowing for example to examine the impact of various design options on the cost, sustainability aspects, and overall performance of the device. This virtual prototyping can further shorten the product development cycle and reduce time to market, thereby increasing the users' competitive edge and leading to cost savings.

The design platform and pilot lines should **operate in a synergistic way** – after virtual prototyping, device designs can be implemented on the pilot lines; the resulting specifications and performances will feed back to designers who can then refine and improve the design models before the next prototype

stage, a **functional demonstrator**, or its transfer to manufacturing. The complete concept and ecosystem is illustrated in figure 42, below.

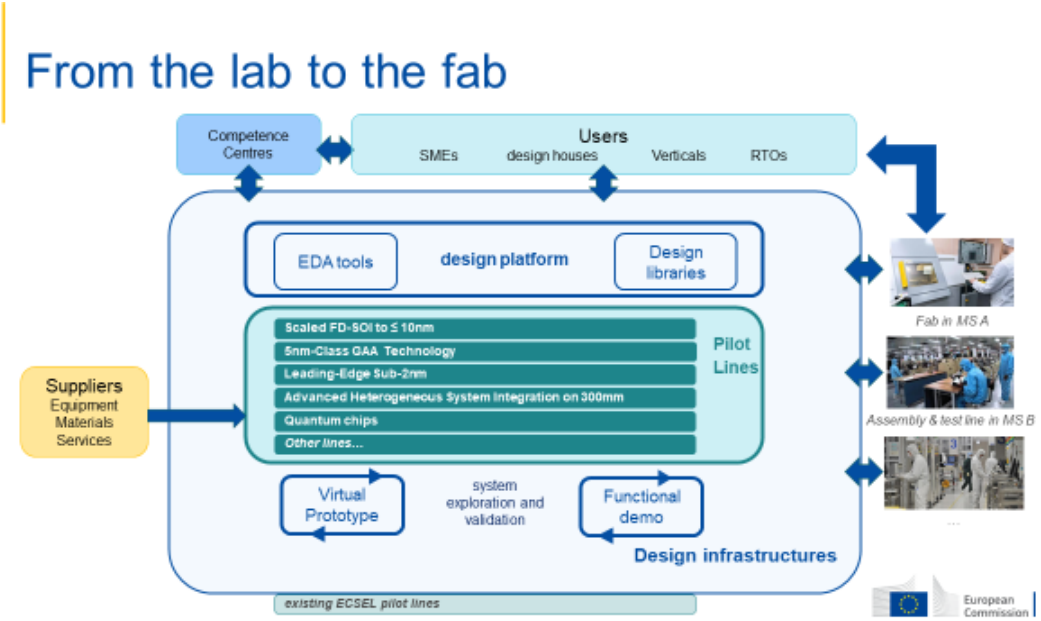


Figure 42. The design infrastructure, pilot lines and relations with users, suppliers and competence centres

Process design kits specific for their technology will be developed by the "owners" of the pilot lines. They can in turn be integrated into EDA tools for use together with libraries of predesigned components to automatically generate the physical layout of new chips. This is a two-way process as issues impacting design are also fed back into the process development to optimize the technology. The availability of these design modules will allow to start chip development cycles even before the full technology is established and ready for yielding production.

Pilot lines allow research to be carried out in an industrial setting but also bring together research activities from various competences, in a way that these bring results that are directly applicable in a production environment. There are currently at least 16 **existing pilot lines** in 10 Member States (see Annex 5). Some of these could be potentially integrated in the design platform infrastructure. The ones addressing the most essential technologies would be integrated first; others could be added according to demand and as the infrastructure is further developed. These were for the most part developed under the ECSEL JU and the Photonics21 public-private partnership[24], and some have already demonstrated technologies from EUV to FinFET and FD-SOI to heterogeneous integration and graphene as well as photonic integrated circuits. Some of these technologies have been taken up by industry and are now on the market.

To date, pilot lines have operated largely separately and independently; by bringing them together in the Chips for Europe Initiative, their complementarities can be exploited in a synergistic way. As mentioned above, process design kits can be developed and reused in new device design as well as libraries that can be shared throughout the design platform.

8.1.4 Investing in competence centres and skills development

[24] www.photonics21.org

A competence centre is a single entity or a coordinated group of entities, with complementary expertise and not-for-profit objectives, capable to support activities in the area of microelectronics and help companies, especially SMEs and small mid-caps, as well as academia, to develop and/or integrate semiconductors in their processes. Competence centres will provide services to facilitate access to pilot lines and to the design platform, provide training and skills development, and support to find investors, make use of existing local competencies and reach out to the relevant verticals. The services will be provided on an open, transparent and non-discriminatory basis.

Once the design platform and associated pilot lines have been put in place, **access** to this infrastructure, virtual facilities and services, must be provided. For this, in each Member State design houses and **competence centres** will be set up to provide access to the tools and libraries and to coach people in how to use the new infrastructure. Linking these through a **network** of competence centres will ensure sharing of information, and local access for users to expertise, to the design platform with its tools and libraries, and to the use of the pilot lines on a pan-European level.

Each competence centre will represent an access point to the European network of competence centres in microelectronics, helping local companies and/or academia to get support from other centres in case the needed competences fall outside their area, ensuring that every stakeholder gets the needed support wherever it is available in Europe. Furthermore, they will connect and be part of the European network of competence centres, European Digital Innovation Hubs (EDIHs) or other innovation ecosystems such as Knowledge and Innovation Communities of the European Institute of Innovation and Technology (EIT KICs), acting as a multiplier for the field of semiconductors and widely diffusing the use of all the microelectronics capacities built up under the Chips for Europe Initiative. Typical entities contributing to the centres will be RTOs or university labs offering technology services, which could work in collaboration with partners whose expertise lies in business development and training. Through these national centres, this networked system will offer unique, world-class innovation capacities in design, virtual prototyping, and design refinement to users. Subsequent real prototyping on the physical pilot lines will provide large scale testing and experimentation of the designed chips and systems with greater and more successful commercialisation provided through reduced costs and a faster route to market. Taken together, this infrastructure and toolset will also facilitate developing and improving the performance and capacities of the more mature technology nodes, which will remain important for many large-scale applications.

The Initiative will provide the R&D community, RTOs, suppliers of technology services, industry, SMEs and start-ups across Europe with ready access to the most advanced technology and design infrastructure. This can be organized in various forms - for example, as cooperation projects with specific focus on building and strengthening the network and with a clear business case in mind. Community interface planes will be set up at several levels ranging from system houses, providers of commercial packaging, testing solutions, application industry to regional competence centres, EDIHs, SMEs and start-ups. Goals are (i) to lower the threshold to access the technology of the pilot lines and fabs; and (ii) to accelerate the design process.

One dimension of the support provided by the competence centres will be the provision of **training** and **development of the necessary skills**, not only in the use of the design tools and infrastructures but also more widely in those required to address the severe skills shortages faced by the EU microelectronics sector (according to the European Commission ICT Monitor, the current number of open vacancies for electronics engineers in Europe is 64 000, and according to the European employment database EURES,

it is more than 320 000[25]). To address this and in order to grow the European ecosystem to meet the goals of the European Chips Act, it is essential to train a workforce. The "Pact for Skills"[26] announced by the Commission in November 2020 set out a new engagement and governance model for mobilising and incentivising stakeholders to make concrete commitments for upskilling and reskilling. It is estimated that more than 250 000 students and workers (from within the sector and coming from other sectors) will need to be skilled/re-skilled across Europe. The number of open positions for engineers and technicians is growing at an alarming rate[27]. The blistering pace of technology calls for rapidly evolving skills in R&D, design, manufacturing, specific applications, AI ethics, cybersecurity, quantum technologies and energy-efficiency. The Chips for Europe Initiative will contribute to building and strengthening the European microelectronics workforce, including through the competence centres which will actively engage with the complete spectrum of education and training providers, with the companies and with the learners. Horizon Europe programmes on skills development and competencies curricula will be complemented by capacity-building in advanced applied digital skills and competences in semiconductor and quantum technologies supported by the Initiative. Moreover, through the Pact for Skills initiative and the Semiconductors Alliance, the Commission will facilitate closer collaboration between industry and academia and the organisation of internships and apprenticeships.

8.1.5 Investing in new pilot lines

Harnessing the existing pilot lines is only the first step and will deliver results for production around 2024-2026. To this infrastructure would be added **new pilot lines** addressing the most advanced technologies to fill the existing gaps in Europe's technological capability and reach the 2030 ambition of being at the leading edge for advanced production capabilities (see Annex 6). These will be developed as research pilot lines to address specific technology challenges, including test and validation. They will have different characteristics in view of satisfying the user requirements, and maximise the successful transfer of results into the industrial environment. The relative involvement of research organisations and industry will depend on the level of technological maturity addressed.

Examples include:

- **FD-SOI at 10 nm and below.** At 22 nm and as already planned at 18 nm, currently FDSOI is the most advanced technology present in foundries and IDMs in Europe. To support their needs and those of the fabless companies using this technology, research and development of further node scaling is required. Much stronger engagement with system companies should also be established to speed up the introduction of new technologies that have similar fabrication requirements, like imaging, photonics, RF, and power, in various applications like IoT, health, and cybersecurity.

- **5 nm-Class Gate-All-Around (GAA) Technology for embedded applications.** A full 5 nm-class GAA technology is to be developed with embedded non-volatile memories and compatibility with 3D stacking, suitable for centralised applications in vehicle electronic architectures, edge computing, 5G/6G infrastructure equipment in telecommunications networks, and industrial automation. This will require to exploit the synergy of process modules already pursued by leading-

[25] https://ec.europa.eu/eures

[26] EU Pact for Skills: upskilling and reskilling initiative for those training and working in the microelectronics industry | Shaping Europe's digital future (europa.eu)

[27] Nearly 1.1 million job advertisements for electro-engineering workers were placed in the EU between mid-2018 and the end of 2019 (CEDEFOP, 2020).

edge nodes like EUV lithography and nanostructured silicon channel integration and will benefit from the research and development efforts on 2 nm leading-edge node GAA technologies.

- **Technology Pilot Line for Leading-Edge Sub-2 nm with a Nanosheet Baseline (<5 nm).** This pilot line will require advanced research and development efforts as it extends beyond existing research line capabilities to deliver modules 'at-pitch' for the next-generation technology nodes as building blocks for the advanced semiconductor roadmap. This will be done in partnership with the semiconductor ecosystem to address Power, Performance, Area, Cost and Environmental impact (PPAC-E) from a system integration point of view, while considering manufacturability and technology insights from the foundries and suppliers. As technology options mature, smooth transfer of know-how will be made in partnership with one or more leading-edge manufacturing partner.

- **Advanced Heterogeneous System Integration Pilot Line on 300mm (AHSI-Pilot Line).** The objective is to offer integration of complex systems (together with R&I, as required) using combinations of different electronic and photonic technologies. This will allow to benefit from the chiplet approach in the industry to integrate advanced semiconductor functionality (manufactured in the most appropriate CMOS technology node). In addition, it will allow to embed new functionalities on chips to enable new sensor applications e.g., for automotive or advanced sensor technologies. Heterogeneous integration of new materials like SiC and GaN will enable very efficient energy conversion (power semiconductors) and wide bandgap semiconductors (SiGe and III/V) will allow very high data rate communication. Additional developments will concern new materials research and engineering for photonic chips and systems.

Although these pilot lines address different technologies, **operating them under a single structure will maximise the synergies between them and bring benefits**: aligning investment in tools and module development; reducing redundancies and improving specialisations in each line; sharing experiences and expertise; providing a single point of contact for prospective users and access to the lines; networked training courses and skills development; and creating a critical mass by bringing together some 10.000 researchers, a portfolio of thousands of patents and high-class cleanrooms.

Other lines may be added in due course. Critical sectors such as Space and Defence may require dedicated pilot lines or priority on pilot lines addressing relevant technologies.

8.1.6 Investing in Advanced Technology and Engineering Capacities for quantum chips

Today, there are no standardised design and manufacturing processes for quantum chips, which are proprietary designs and in essence hand made. For large-scale uptake and mass-market applications, it is necessary to develop such standardised processes. As the underlying materials and structures are in most cases similar to traditional microelectronics or photonics, the design and manufacturing process of quantum chips need to be aligned with those of the traditional semiconductor industry. This would have the additional benefit of facilitating integration of the quantum device with the control electronics, connectivity, etc., necessary for the quantum devices to work, but now missing and largely external to the quantum chip.

The European Commission has therefore proposed to complement, in the Chips for Europe initiative, the activities it is already financing under Horizon Europe's Quantum Technologies Flagship. The Chips for Europe initiative would thus focus on the specific needs of the future generation of information processing components exploiting non-classical principles, notably chips exploiting quantum effects (i.e. quantum chips) based on research activities, notably by investing on (a) Innovative

design libraries for quantum chips; (b) quantum pilot lines; and, (c) testing and experimentation facilities.

- **Innovative design libraries for quantum chips:** The aim is to align the design and fabrication processes of quantum chips with the well-established and standardized processes of the classical semiconductor industry. This should not only accelerate the capability of the Union to mass-manufacture in a reproducible way quantum chips but will also facilitate the integration of the quantum devices as sensors or processors within the classical microchips. This should be complemented by the development of standardised design libraries and fabrication processes for the quantum chips that are not compatible with semiconductors, but are relying for example on nanostructures.

- **Quantum Pilot Lines:** The Quantum Technologies Flagship Initiative, with the support of the RTOs, is establishing the first quantum pilot lines to bring together the different and proprietary quantum chip design and fabrication processes to achieve harmonisation and compatibility with the existing manufacturing infrastructures. This should bring the design and fabrication of quantum components closer to the well-established processes of the classic semiconductor industry, for all semiconductor- and photonics-based qubit platforms. This will lead to a miniaturisation of the quantum chips, and a higher integration density. Under the Chips Act those emerging quantum pilot lines will be integrated with the relevant semiconductor pilot lines in view of further maturation, and to develop the mass-manufacturing capability. It will also address the integration of quantum components as chiplets in semiconductor microchips. For the alternative qubit platforms, that are not compatible with semiconductors, the quantum pilot lines will form part of the advanced pilot lines to be operational by 2026 – 2027.

- **Testing and experimentation facilities:** The pilot lines will also provide access to testing and experimentation facilities where tailor made quantum components can be tested, including the components produced by the pilot lines.

In addition to the above, the semiconductor competence centres will bring together designers, producers and users of quantum components to develop the next generation(s) of quantum devices as stand-alone quantum chips, or as quantum devices integrated in the classical microchips.

8.1.7 Managing the Intellectual Property

As an overall principle, Intellectual Property (IP) rules should maximize the opportunity to enter the market by deploying foreground IP for specific product-market combinations. In this spirit, where needed and feasible, background IP should be made available to other consortia members in order to facilitate the exploitation of foreground IP. With regard to the set-up of pilot lines, general principles will need to be established up-front that allow co-ownership in the cases of co-invention, and shared IP rights when sharing risks and investments.

Process technology IP should enable technology transfer at a later stage. Exclusive IP rights in certain partner-product-market combinations may be warranted, guided by specific conditions - for instance, in the case of exclusive contributions to associated R&D. For example, this can be the case with contributions from the users, and in case of spin-offs, start-ups being generated. The overall aim is to enable open IP platforms in Europe for rapid growth.

These general principles should allow partners to collaborate on R&D challenges and also focus efforts towards developing prototypes. They should also recognize that in breakthrough research phases, more

generically applicable results will be achieved that allow for more flexible and broader sharing arrangements than when approaching the prototype phase where application- and partner-confidential information will necessarily apply.

8.1.8 Implementing the Chips for Europe initiative: the Chips Joint Undertaking

The Chips for Europe Initiative as outlined above would be implemented via the Key Digital Technologies Joint Undertaking (KDT JU), which would have its scope enlarged in terms of types of activities supported, and its name changed to '**Chips JU**'. This would build upon the strong knowledge base acquired by the ECSEL JU and its successor, the KDT JU. The KDT JU was one of the nine JUs set up by the so-called 'Single Basic Act'[28]. The change from the ECSEL JU under Horizon 2020 to the KDT JU under Horizon Europe led to an adaptation to the changing geopolitical situation and continued technological convergence. The scope was extended, going beyond microelectronics to relevant aspects of photonics, beyond embedded software to relevant higher layers of software, beyond Smart Systems to enable intelligent Systems of Systems (SoS), and addressing important trends including the emergence of new computing paradigms, edge-computing and its link with cloud computing – in particular for AI applications[29].

The Chips JU would have the responsibility for the implementation of four components of the Chips for Europe Initiative, namely:

- design capacities for integrated semiconductor technologies;
- pilot lines for preparing innovative production, and testing and experimentation facilities;
- advanced technology and engineering capacities for quantum chips; and
- a network of competence centres and skills development.

The fifth component of the Chips for Europe Initiative, the 'Chips Fund', would not be implemented by the Chips JU.

The amendment of the Single Basic Act (SBA), would add capacity building activities to the research and innovation activities currently supported by the KDT JU. Whereas the SBA set up the KDT JU, defined its objectives, bodies, and governance, and laid down the provisions to ensure a smooth transition from its predecessor, the SBA amendment makes relatively minor changes to prepare the KDT JU for the implementation of the Chips for Europe Initiative, to adjust its governance accordingly, and to introduce capacity building activities. Such activities would strengthen and promote Europe's capacities in semiconductor areas through large-scale deployment. Capacitiy building activities under the Chips JU would be funded via the Digital Europe Programme and would be limited to the four components of the Chips for Europe Initiative; they would not cover the full scope of the current KDT JU.

In addition, the Chips Act and the SBA amendment would increase the support for the JU's research and innovation activities, funded via Horizon Europe. It should be noted that many activities that would be considered research and innovation activities on the four components of the Chips for Europe Initiative are currently supported by the KDT JU and previously by the ECSEL JU. Examples are

[28] Council Regulation (EU) 2021/2085 of 19 November 2021 establishing the Joint Undertakings under Horizon Europe and repealing Regulations (EC) No 219/2007, (EU) No 557/2014, (EU) No 558/2014, (EU) No 559/2014, (EU) No 560/2014, (EU) No 561/2014 and (EU) No 642/2014.
[29] See draft partnership proposal for the Key Digital Technologies Joint Undertaking, in particular section 2.2.5. https://ec.europa.eu/info/files/european-partnership-key-digital-technologies-kdt_en

research and innovation activities on pilot lines supported by ECSEL (see Annex 5 for detailed examples) and the development of open-source RISC-V building blocks under KDT Work Programme 2021[30].

Apart from the introduction of capacity building activities for the four components of the Chips for Europe Initiative, coverage of the Chips JU would not be substantially different from that of the KDT JU. Decisions on adjusting scope in work programmes of the Chips JU would follow the governance rules as outlined in the SBA amendment (see also Chapter 9).

Given the importance of the semiconductor sector for downstream industries (see e.g. Section 2.4), it is expected that the Chips JU will take advantage of synergies with other European Partnerships. The Chips JU, for example, would be well positioned to cooperate with partnerships in mobility, e.g. on the development of chips and control systems for autonomous vehicles[31]. Similarly, cooperation could be established with partnerships in energy, health, agriculture, and other industrial sectors. In addition, cooperation with other digital partnerships is expected.

The Chips JU was proposed to have a total Union contribution of EUR 4.175 billion and a commensurate contribution by Participating States. Further explanation and details are provided in Chapter 10 and the legislative and financial statement (LFS) accompanying the proposed Chips Act.

8.1.9 The role of the European Chips Infrastructure Consortium (ECIC)

The Chips Act introduces the possibility to establish one or more European Chips Infrastructure Consortia (ECIC) – a mechanism to facilitate the implementation of different parts of the Chips for Europe Initiative, including for example the set-up of the new pilot lines. The main aim of an ECIC is to encourage effective and structural collaboration between legal entities, including Research and Technology Organizations and Member States. To enhance collaboration, the ECIC has to involve the participation of at least three legal entities from three Member States (these legal entities could be Member States themselves).

The use of the ECIC instrument offers several advantages over existing instruments in terms of autonomy, flexibility, and duration. An ECIC would have legal personality, and sufficient autonomy to lay down its membership, governance, funding, budget, the modalities by which the respective financial contributions from the members are called upon, and coordination, management and working methods. The members of the consortium would have full flexibility in determining applicable law, statutory seat, voting rights or any other incorporation or operational legal provisions as long as the proposed set-up would not contradict the conditions of the Chips for Europe Initiative and the objectives of the Chips Act. The process to set up an ECIC is set out in Article 7 of the Chips Act: the coordinator would submit an application to the Commission; the Commission would review the application based on the conditions provided in the Chips Act and if all conditions are met, adopt an implementing act setting up the ECIC. The Commission would not be part of the ECIC Consortium.

The ECIC would implement one or more activities foreseen by the Chips for Europe Initiative, for example the new pilot lines. For this, the Chips JU would launch a call for expression of interest, calling for an ECIC to implement the specific activity. The ECIC would receive budget from the EU and

[30] The resulting IP libraries could be part of design capacities for integrated semiconductor technologies. For the KDT Work Programme 2021, see https://www.kdt-ju.europa.eu/wp2021.
[31] The connected, cooperative & automated mobility (CCAM) partnership would be an appropriate partnership for such cooperation.

interested Member States to be shared and implemented on the basis of the particular ECIC setup and in line with State aid rules; the exact procedure for doing so would be established by the ECIC itself.

The procedure and the details for the expression of interest of an activity to be implemented by an ECIC are not provided in the proposed Chips Act nor in the amendment to Regulation 2021/2085 establishing the Joint Undertakings under Horizon Europe (Single Basic Act, 'SBA'). This would have to be decided in the Work Programme of the Chips JU as an implementing body of the Initiative.

In this call for expression of interest, the ECIC would be asked to apply in order to implement the specific activity under the Initiative, by providing among others the following: a technological roadmap, the financial construct of the activity, including the Union contribution, the implementing partners, the implementation timeframe, the general rules for the IP policy on which the ROI could be carried out. If the ECIC is selected, it will become the implementing entity of the specific activity of the JU's work programme.

The mechanism provided by ECIC has a number of advantages over other instruments such as a JU. Firstly, it allows to **combine funding** from Member States, the Union and from the private sector, including throughout **a longer timeframe than the current Multiannual Financial Framework (MFF)**. Secondly, having legal personality, an ECIC could also engage in the **contracting of loans** (for example, through the EIB), to be repaid through revenue-generating activities such as IP creation and pilot lines' services. Thirdly, the ECIC could **own the infrastructure** and develop and **manage its intellectual property.** This could attract new business players; e.g. pilot lines may develop IP that would be essential for future production facilities or support the preparation of production nodes below 2 nm, strengthening collaboration with the First-Of-A-Kind production facilities foreseen in Pillar II of the Chips Act. Additional Member States and private partners could join the ECIC and financially contribute to its activities over time; Member States' contributions to the ECIC will be counted as national contributions to the JU. **A single ECIC would give further advantages**: maximise the synergies between the constituent pilot lines and the resulting benefits outlined above as in more power in purchasing tools and module development; reducing redundancies in operations; sharing experiences, libraries and IP; offering a single point of contact and legal entity in operating the lines; and creating a single, shared resource with critical mass by pooling the resources of all participants.

The ECIC implementation roadmap can adopt a phased approach to project development i.e. the first phase focusing on research aspects, equipment and other developments necessary for establishing the new pilot lines, followed by the second phase of their operationalisation and service provision. This phased approach would guarantee that the required budgets would be made available by the Member States and any private sector participants during the projected period of the pilot line operation, thus respecting the timeframes for implementing these pilot lines.

8.1.10 The Chips Fund

To develop a thriving semiconductor ecosystem, easier access to finance and investment opportunities for SMEs are needed. Overall, start-ups and scale-ups represent an important source of innovation, and their growth is essential to fuel a dynamic and forward-looking ecosystem. In Europe, innovative deep-tech semiconductor SMEs (including the ones addressing quantum technologies) face financing challenges over a long period, before returns are generated. Fabless companies incur into substantial costs for development, licensing IP and tools, prototyping and contract manufacturing, before they can generate any revenues, and without adequate financial support, they are often vulnerable to foreign acquisitions or brain-drain.

Financing these semiconductor companies requires an understanding of the characteristics of the industry and the needs for significant investments with a longer-term horizon. To address this need, a dedicated semiconductor investment facility was proposed to be established in the Chips Act package: **the Chips Fund**. This would provide increased availability of loans, venture capital financing and specialised funds, including equity investment solutions created through targeted investment facilities with the participation of the European Investment Bank (EIB) group, other financial institutions and private equity partners.

Firstly, for high-potential start-ups needing support to validate their technology and transform it into innovation, the **EIC** (European Innovation Council) **Accelerator** programme of Horizon Europe will offer a thematic challenge in the area of semiconductor technologies and quantum chips. This instrument will deploy up to EUR 300 million, potentially generating a multiplying effect of a factor 3 in private investments, addressing early investment gaps in the form of grants and equity, to help start-ups generate novel IP and mature their technology, thereby attracting further investors.

Secondly, for SMEs requiring financial support to scale-up their efforts and bring innovation to market, the **InvestEU Fund**, will offer dedicated financial products to be implemented by the EIB Group, International Financial Institutions and national promotional banks (NPBs) through financial intermediaries, such as venture capital or private equity funds. A dedicated budget to support investments in semiconductor chips and technologies will secure a guarantee of up to EUR 250 million, , for funding companies playing a role in the semiconductors value chain, from technology development to design and system integration, which is expected to leverage about EUR 1.2 billion of equity-based financing with other market investors.

Further, in the InvestEU Guarantee agreement with EIB Group, semiconductors are identified as an area of priority for investment. The EIB is ready to provide substantial resources in the form of loans and venture debt to support projects in line with EU ambitions, such as in the area of manufacturing, pilot lines, and technology infrastructures.

8.1.11 Impact and benefits

Establishing a technology infrastructure based on a model of openness and inclusiveness as described above will **accelerate the flow of innovation** and **strengthen the microelectronics ecosystem** in Europe. It will provide the stakeholders (see below) with **easier and faster access** to the design and piloting infrastructure. The work will be organized in the form of a series of intimately connected projects with specific focus, well-defined interactions and with a clear business case in mind.

The technology infrastructure, through the involvement of competence centres and the EDIHs, will act as an **aggregator of customer requests** (in particular from SMEs and start-ups) and bundle them into runs in pilot lines or commercial fabs. The direct benefits will be (i) **substantially lower costs** of accessing the technologies being piloted; and (ii) an **acceleration of the innovation cycle** with seamless design, prototyping and manufacturing processes resulting in faster development of products.

Emerging design solutions, such as ultra-low-power energy-efficient processors, or processors and accelerators for different vertical sectors based on the open-source RISC-V computing architecture, will be tailored for feeding into sectors including automotive, energy, and medtech. The R&I activities would lead to IP blocks that could be part of libraries that would become an essential component of the design platform.

For the pilot lines, research and innovation activities would develop – for example – technologies to achieve transistor sizes below 2 nm, novel materials, as well as heterogeneous and 3D integration of

different materials. Such R&I activities could be performed together with ongoing research on advanced materials, thereby contributing to HE Cluster 4 objectives.

Finally, by validating new processes before transfer to IDMs, the new pilot lines will enable participating companies to **commit to invest in the next generation of chips**, as outlined in articles 10 and 11 of the Chips Act.

In summary, the **specific benefits for European stakeholders** expected from Pillar 1 are:

- ***SMEs and start-ups*** will have **easier and faster access to foundry services** via a single point of contact, and lower development costs due to support in design and system integration and the use of cost-efficient options such as multi-project wafer (MPW) runs.

- ***Industry users and product developers*** will have **easier use of design tools and libraries** as well as **early access to advanced technologies**, through pilot lines for testing and experimentation and through foundries for volume manufacturing and heterogeneous integration. They will be enabled to **design innovative components and new system concepts** and **demonstrate key functionalities** such as new approaches to high performance, low energy, security, new 3D and heterogeneous system architectures, etc.

- ***Researchers*** will have access to and the use of **advanced facilities for developing, testing and refining** new technology concepts and prototypes.

- ***Equipment manufacturers*** will **develop, validate and demonstrate** their latest models in an advanced pre-production environment.

- ***Design companies*** will have **access to design libraries** and, through the pilot lines, be able **to develop and refine their EDA tools and IP** for advanced technologies and at leading edge nodes, thereby increasing their own product portfolio and businesses.

- The ***European ecosystem at large*** will be more easily **address their needs and requirements** and have wider, democratized **access to highly developed and expensive technologies** for key sectors such as automotive, industrial automation, communications, and healthcare, and **improved support by lowering the barrier to prototypes** and enabling small volume production, as well as opportunities and facilities for skills development and **developing a trained workforce** (see 8.1.4 above).

8.2 Pillar 2. A Framework to Ensure Security of Supply

8.2.1 Urgency to invest in new production capabilities for the EU

The supply chain disruptions and the shortages addressed in chapter 2 are symptoms of **the EU's excess dependency on production capacities located in third countries.** The EU's share of the global production capacity has been declining over the past 20 years. Moreover, the EU currently has no foundries that offer advanced manufacturing of components with feature sizes below 22 nm while the majority of capacity in the EU is still concentrated at 28 nm and above. The EU thus relies on imports for chips (for both leading-edge and mature nodes) that are then embedded in products manufactured by its industries, including automotive. In 2021, the EU exported semiconductors for a value of EUR 31.5 billion and imported for EUR 51 billion, i.e. with a deficit of EUR 19.5 billion (section 3.2).

Sections 3.2 and 3.3 illustrate the limited investments in the EU in the semiconductor sector (with about 4% of global capital expenditures since 2010 – see figure below). This led to a situation where the EU now only has a share of manufacturing capacities (7.2% of global market share in 2020) which is not commensurate with its economic weight and the needs of its industries. This exposes the EU to excessive dependencies.

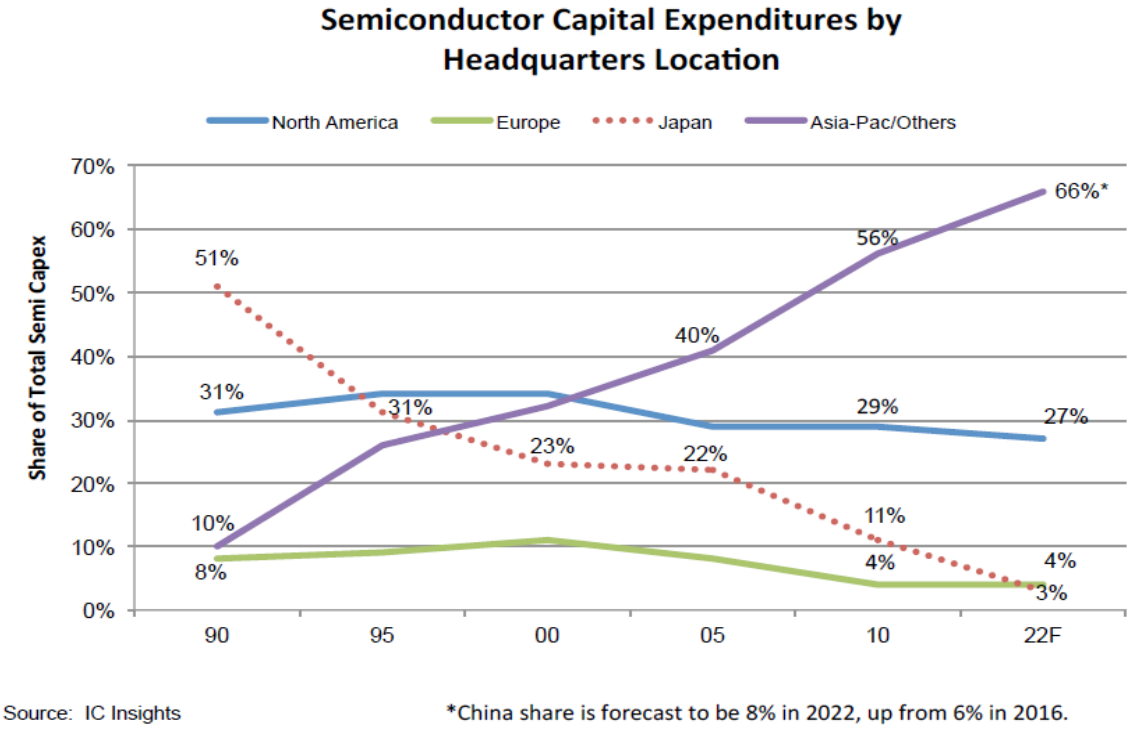


Figure 43. Evolution of capital expenditure in semiconductor sector by region (based on headquarters location – Source IC insights 2022)

Limited investment in production capacity is a consequence of the high costs and complexity of production of chips, which increase as chips become more advanced, and of an uncertain business model (see section 1.2.1). A leading-edge fab typically requires an investment of several billion euros. Taiwan and South Korea currently are the only countries in the world with leading-edge manufacturing capacities covering node sizes smaller than 5 nm and below. The fabs now active in the EU only produce advanced and mature nodes, whereas the application of cutting-edge chips in the future is expected to increase across many application areas. This will notably concern critical sectors (such as health,

transport or energy) and sectors which can still be considered as European strongholds (such as automotive) (see Chapter 4).

As semiconductors have clearly become a **strategic technological area**, the EU needs to **reinforce its capacity in the production of mature nodes** (10 to 28 nm), essential for the functioning of its economy, while at the same time **preparing for investing in production of nodes smaller than 10 nm**, which offer significant growth potential. Technological advances also need to be fostered on other important aspects than miniaturization, such as the use of innovative materials or processes or, for example, the improvement of chips manufacturing circularity (water consumption and reuse, and energy-efficiency) (see Chapter 5).

Furthermore, in view of the time needed to develop, build and setup manufacturing capacities, **it is of the utmost importance to invest now.** Today's efforts will shape the type and scale of production capacity available in the EU in 2030. A semiconductor fabrication plant typically requires two years to build and another one to two years to optimise production processes. Investments now will allow increasing production capacity in the EU as of 2025-26 in more mature nodes. And investments now in leading-edge nodes, starting with advanced pilot lines, are needed to develop knowledge and skills and be able to translate such investments in new production capabilities at 2 nm or below around 2028-2030 in Europe.

Without rapid and sufficient investments, Europe's market share could drop to less than 5%, given the doubling of the market and the scale of efforts taking place now in other parts of the world. **In the very recent years, the governments of China, the United States, Japan and South Korea took measures to support through incentives their local industrial ecosystems.** These countries support their chips industry with direct subsidies, tax exemptions, preferential customs and tariffs treatment, tax incentives to support innovation, investment funds, and regulatory action[32]. As part of the 'Made in China 2025' plan[33], the Chinese government allocated USD 150 billion over ten years to the sector with the ambition to reach 70% of self-sufficiency by 2025. The US Chips Act[34] should provide USD 52 billion of subsidies to support investments in R&D and semiconductor manufacturing in the United States until 2026. South Korea plans to support its semiconductor industry through tax incentives for its domestic companies' private investments in R&D and manufacturing, which are estimated to total USD 450 billion until 2030[35].

In view of the very high and still increasing capital intensity of the semiconductor manufacturing sector[36], private investment may likely require public **support with a view to achieving EU's ambition to reach 20% of global market share by value in leading edge semiconductors**[37] and **ensuring access to green, secure and trusted chips in Europe.**

With a framework for facilitating the establishment of **first-of-a-kind facilities**, the actions proposed under the second pillar of the Chips Act aim at contributing to **the EU's security of supply and strengthening of a resilient semiconductor ecosystem.** The expected resulting effect on production

[32] https://www.institutmntaigne.g/essuces/dfs/ublicatins/eue-new-gelitics-technlgy-1.df
[33] https://csets.cngess.gv/duct/df/R/R46767
[34] https://www.cngess.gv/bill/117th-cngess/senate-bill/1260?s=1&=52
[35] https://sectum.ieee.g/suth-keas-450billin-investment-latest-in-chi-making-ush
[36] The CAPEX as a percentage of the semiconductor market has significantly increased between 2010 and 2021, from 13.83% to 25.37%.
[37] See COM(2021)118 – 2030 Digital Compass: the European way to the Digital Decade.

capacities in Europe should also help ensure the security of supply of leading-edge components in particular while these are likely to become essential to many sectors (see Chapter 4).

The EU aims to be able to master and develop technologies that are pervasive to its digital economy. Advances concern performance but also energy-efficiency, security and data protection: the **development of more sustainable, trusted and secure chips** is an important objective of the pillar.

Leading-edge manufacturing capacities, including related foundry activities, are expected to have a positive impact on the pan-European ecosystem, stimulating the further development of fabless (or fab-lite) companies, advanced equipment and material suppliers, as well as fuelling the activities of RTOs. This should also be conducive to creating, retaining and attracting talents throughout the EU.

8.2.2 Explaining further the pillar 2 approach

The Chips Act proposes a framework to facilitate the implementation of projects that contribute to the security of supply and strengthen the resilience of the semiconductor ecosystem in the EU. Private investment in these facilities will likely require significant public support. Focusing public support on innovation is essential to ensure the longevity of public investment and limit the distorting effect on competition. Innovation could be recognised in different dimensions, ranging from process to product to energy performance. The Chips Act defines the concept of "first-of-a-kind facility in the Union" to provide guidance how such innovation should be demonstrated for the purpose of the Chips Act, i.e. in order to be recognised as an "Integrated Production Facility" or "Open EU Foundry". The Commission has already announced in the Communication "*A Chips Act for Europe*"[38] that it will also take this element into account for a possible State aid approval based on Article 107(3)(c) TFEU.

Under Article 107(3)(c) TFEU, the Commission may consider aid to facilitate the development of certain economic activities or of certain economic areas to be compatible with State aid rules, where it does not adversely affect trading conditions to an extent contrary to the common interest. To assess whether the aid does not adversely affect trading conditions, the Commission weighs the positive effects of such State aid against its likely negative impact on trade and competition for each individual case. Such positive effects include "pan-European" factors, such as a positive impact on the semiconductor value chain with regard to ensuring the security of supply and increasing qualified workforce, or its positive impact on the innovation potential of SMEs and verticals that can access innovative products at their doorsteps, or any other benefit that can be shared widely and without discrimination across the EU economy. As part of this overall balancing, the Commission will take into account that a new production facility is "first-of-a-kind" in the Union.

Under the proposed framework of the Chips Act, semiconductor manufacturing facilities would be able to receive a label that determines that these are "first-of-a-kind" facilities in the Union. The framework includes provisions to facilitate the establishment and operation, while requiring that these projects comply with criteria to ensure they contribute to the objectives and that they remain a reliable supplier of chips in a crisis. The two separate procedures for the recognition and for authorisation of State aid, where applicable, will be conducted in parallel (see the section 'Procedures' below).

[38] COM(2022) 45 final. See also the Questions and Answers available at https://ec.europa.eu/commission/presscorner/detail/en/QANDA_22_730

First-of-a-kind facility in the Union. In order to address the market failures as laid out above (see section 8.2.1), the Commission announced that it may authorise public support for the establishment of "first-of-a-kind" facilities in the Union.

This approach will be fully complementary to existing frameworks based on Article 107 TFEU and does not limit further possibilities to grant State aid, where these would also apply to the project in question. It is in particular complementary to the framework of Important Projects of Common European Interest (IPCEI) based on Article 107(3)(b) TFEU, which is intended to support multi-country R&I projects up to first industrial deployment in areas of common interest, thus supporting a different stage of the innovation cycle.

The Chips Act provides for a definition of such a "first-of-a-kind" facility. According to Article 2 (10), this would be defined as "an industrial facility capable of semiconductor manufacturing, including front-end or back-end, or both, that is not substantively already present or committed to be built within the Union, for instance with regard to the technology node, substrate material, such as silicon carbide and gallium nitride, and other product innovation that can offer better performance, process innovation or energy and environmental performance".

In essence, to be recognised as first-of-a-kind, a facility would need to offer a dimension of innovation that is not yet present in the EU. This innovation could be, for example, with respect to process, product or performance. This applies to projects for any production node, whether leading-edge or not. The definition provides an indicative list of these qualifying factors, e.g. the use of novel substrate materials such as silicon carbide and gallium nitride, smaller nodes, new functionalities or environmental performance of the chip. Innovation can be recognised in different dimensions. A suitable reference to identify the areas where such innovation can take place is the IEEE International Roadmap for Devices and Systems (IRDS), which identifies key technological trends related to devices, systems and all related technologies.[39]

A manufacturing facility of a comparable innovation capability should not yet be **substantively present** or committed to be built in the EU. This means that a manufacturing facility capable of producing a comparable product, process or performance at an industrial scale should not yet exist or currently be under establishment in the EU. In turn, if such innovation was already in use in R&D or small-scale production in the EU, this would not necessarily exclude new mass production qualifying as "first-of-a-kind". For instance, a manufacturing facility planning to use a novel substrate material could qualify as "first-of-a-kind" in the EU, despite this substrate material being tested in a pilot line in a Member State.

In this respect, it should be noted that it is not excluded that several parallel projects may be recognised as first-of-a-kind if each of them does not crowd out existing or planned private activities and if there is no risk of overcapacity.[40]

Framework for a label for "first-of-a-kind" facilities. To encourage investments in new production capacity, while at the same time ensuring these are to the benefit of the EU as a whole, the Chips Act

[39] This builds on the previous work of the ITRS, which also defined the reference for the process nodes (in nanometres) resulting from the evolutions of transistor scaling, in line with the prediction of Moore's law. The IRDS currently includes work by different International Focus Teams on the following fields: More Moore (scaling); More than Moore; Beyond CMOS; Systems and Architectures; Packaging Integration; Outside System Connectivity; Cryogenic Electronics and Quantum Information Processing; Lithography; Yield enhancement; Metrology; Factory Integration; Environment, Safety, Health, and Sustainability.

[40] See footnote 56 of the Communication, A Chips Act for Europe, COM(2022) 45.

proposes a framework for the implementation of two types of "first-of-a-kind" facilities. These two types reflect the two common business models of semiconductor manufacturing facilities in today's semiconductor industry landscape.[41] **Integrated Production Facilities (IPF)** are vertically integrated semiconductor manufacturing facilities, which are involved in front-end manufacturing[42] as well as in the design of integrated circuits or the provision of back-end services[43], or both. **Open EU Foundries (OEF)** are semiconductor manufacturing facilities which dedicate at least a certain extent of their production capacity to produce chips according to the design of other companies, in particular fabless companies. The framework proposes that companies could apply to the Commission to receive the label of Integrated Production Facility or Open EU Foundry for their planned facility.

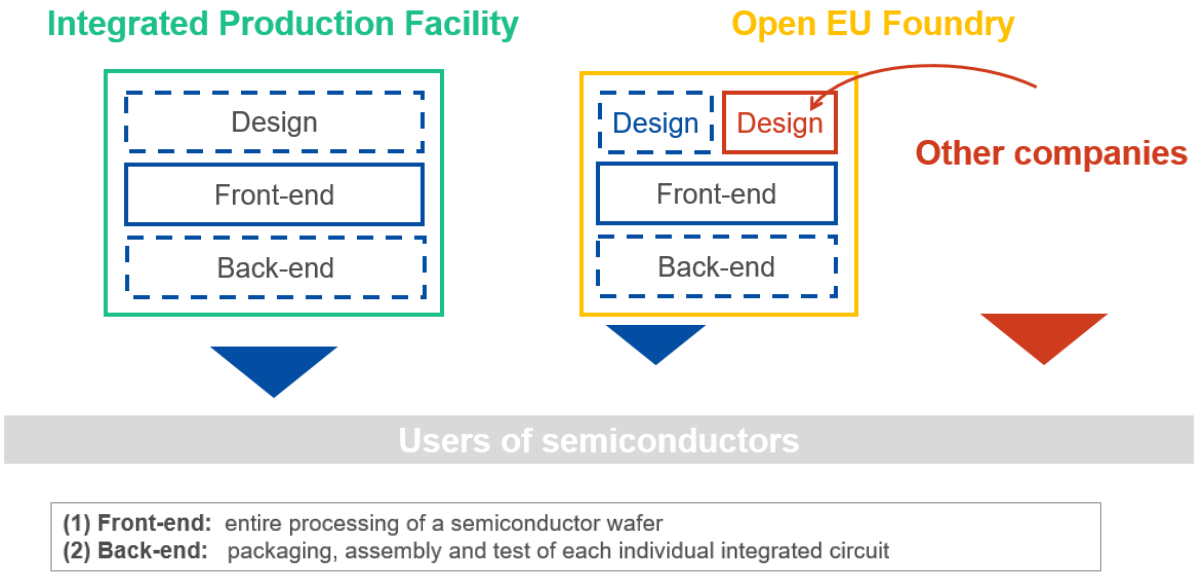


Figure 44. Comparison of the business models for Integrated Production Facilities and Open EU Foundries.

Criteria to ensure security of supply. To achieve the objective of increasing security of supply and strengthening the resilience of the EU's semiconductor ecosystem, these facilities would have to comply with certain criteria in order to qualify for the label. The purpose of these criteria is to ensure that these facilities contribute to the objectives, as well as to ensure they remain a reliable supplier in a shortage crisis.

- First, their establishment and operation would need to have a **clear positive impact on the Union's semiconductor value chain** with regard to contributing to the security of supply and increasing qualified workforce. The impact on the EU's value chain would be considered on a case-by-case basis.
- Second, they would have **to guarantee not to be subject to the extraterritorial application of public service obligations of third countries** in a way that may undermine the

[41] For an overview of the prevailing business models in the semiconductor industry, please refer to Section 1.2 (Global Semiconductor Value Chain).
[42] 'Front-end' means the entire processing of a semiconductor wafer (Article 2 paragraph 12). The front-end manufacturing activities by Integrated Production Facilities or Open EU Foundries could cover one or all steps in the processing of a semiconductor wafer, starting from various substrate materials (Si, SiC, SOI…).
[43] 'Back-end' means the packaging, assembly and test of each individual integrated circuit (Article 2 paragraph 13).

undertaking's ability to comply with their obligations under the Chips Act[44]. Hence, if Integrated Production Facilities or Open EU Foundries could expect to be subject to a public service obligation from a third country as well as a conflicting obligation from the Commission, they would be requested to organise their production capacity and sequence in a way to ensure the obligations imposed by the Commission can be fulfilled. Such guarantee could for instance be given via written statement and would need to include the commitment to inform the Commission if such instance arises.

- Third, they would need to provide a **clear commitment to invest in the next generation of chips**. Such a commitment could entail, for example, the commitment to contribute to the implementation of pillar 1 through providing knowledge and skills in preparing pilot lines, closely following and contributing to the development of those. Equally, the content of such a commitment could be having a pre-production facility installed in their facilities, for taking the results of the pilot line effort from the lab (e.g. the RTO) to the fab. The commitment could be demonstrated through preparing to invest in more advanced technological nodes (improving computing power and energy efficiency) or contributing to the preparation of pilot lines, or having pre-production facilities on their premises etc.

Benefits of receiving the label. Companies or consortia of companies could apply to the Commission to recognise their initiative as Integrated Production Facility or Open EU Foundry. This would lead to receiving the label as either type of facility. This is a separate procedure to the State aid assessment and, where applicable, these two procedures would be conducted in parallel. Receiving the label would entail several benefits:

- First, the Chips Act provides for **a streamlined approach to administrative applications**. These provisions are designed to address typical barriers to the implementation of large scale semiconductor manufacturing facilities, pertaining to the extensive time required for projects to acquire administrative permits and complex and fragmented permit-granting processes.

  Under Article 14, projects with the label would benefit from fast-tracking of administrative applications, such as environmental assessments and spatial planning. Where possible under national administrative law, they would be allocated a priority status. Furthermore, the Chips Act provides that the security of supply of semiconductors may be considered an imperative reason of overriding public interest within the meaning of Article 6(4) and Article 16(1)(c) of Directive 92/43/EEC (the "Habitats Directive") and Article 4(7) of Directive 2000/60/EC (the "Water Framework Directive"). The aforementioned directives allow in exceptional circumstances that projects may be implemented despite receiving a negative environmental assessment, if certain conditions are fulfilled and there is an imperative reason of overriding public interest[45]. The proposed provision in the Chips Act would clarify that the planning,

[44] Integrated Production Facilities and Open EU Foundries could be obliged to accept and prioritise certain orders for critical sectors in line with Article 21 paragraph 1 of the proposal (see section 8.3.3).

[45] For instance, Article 6(3) of the Habitats Directive requires appropriate assessment ("AA") of plans and projects that are likely to impact a Natura 2000 site. By way of derogation from the provisions of Article 6(3), a planned facility could be authorised for which the AA concludes a negative assessment of the implications for the site in view of its conservation objectives. In this case, the deciding authority would have to establish that all conditions of paragraph 4 of this Article, which is providing for the possibility to derogate, are met. This requires that no alternative solutions are available and that the facility is necessary for 'imperative reasons of overriding public interest'. It would also be necessary to demonstrate that compensation measures, which ensure that the overall coherence of the Natura 2000 network is maintained, have been secured. Article 14 paragraph 3 of the Chips Act proposes that the security of supply of semiconductors could be such an 'imperative reason of overriding public interest'. Since Integrated Production Facilities and Open EU Foundries would be considered to contribute to the

construct and operation of Integrated Production Facilities and Open EU Foundries may be considered as being of overriding public interest in this context. This consideration is given in light of the importance semiconductor technologies, and more generally digital technologies, have as enablers for the sustainability transition.

Furthermore, the Chips Act requires Member States to implement a **'one-stop-shop' approach to permit applications** and enhance coordination of the administrative process (Article 14 paragraph 4). For this purpose, Member States should nominate an authority responsible for facilitating and coordinating all administrative applications related to planning, construction and operation of each Integrated Production Facility and Open EU Foundry. Such a nomination becomes necessary for each project after it has received the label. The approach to provide the above-described benefits of fast-tracking of administrative applications and a 'one-stop-shop' for administrative applications follows the example of another EU policy area: the Regulation on the guidelines for trans-European energy infrastructure[46] grants certain administrative benefits and foresees the possibility to derogate from EU environmental directives for key energy infrastructure projects. The list of these key energy infrastructure projects is updated by the Commission through a delegated act every two years. Most recently, such a proposal was adopted in November 2021.[47] The new list consists of 98 projects in the areas of electricity transmission and storage, smart grid deployment, gas, and cross-border carbon dioxide networks.

- Secondly, Integrated Production Facilities and Open EU Foundries would receive **priority access to the pilot lines set up under the Chips for Europe Initiative**, meaning, for example, that their application to use the pilot lines could be accelerated and preferentially treated, without excluding or preventing effective access by others.
- Thirdly, receiving the label would **determine that a facility is "first-of-a-kind" and contributes to the security of supply in the Union**. Separately, the Commission will also take this element among others into account in the possible State aid procedure based on Article 107(3)(c) TFEU, as announced in the Communication "*A Chips Act for Europe*".

Procedure. For the recognition of their (planned) project as Integrated Production Facility or Open EU Foundry, individual companies or a consortium of companies would be able to apply directly to the Commission. The assessment would consider compliance with the criteria for Integrated Production Facilities or Open EU Foundries and the viability of the project. For the latter, the proposal suggests that applicants submit the business plan evaluating the financial viability of the project, documentation of the experience of the applicant and a letter proving the readiness of the Member States(s) on whose territory the facility would be built to facilitate its set-up. This documentation would enable the Commission to target the label to projects with a demonstrated prospect of success. After an initial assessment of the submitted documentation, the Commission would consult the European Semiconductor Board, which is an advisory body established in the Chips Act and consisting of representatives from the Member States (see Chapter 9). If the Commission's assessment is positive, it would approve the recognition by a decision.

security of supply of semiconductors, their planning, establishment and operation could provide grounds for such a derogation.

[46] Regulation (EU) No 347/2013 of the European Parliament and of the Council of 17 April 2013 on guidelines for trans-European energy infrastructure and repealing Decision No 1364/2006/EC and amending Regulations (EC) No 713/2009, (EC) No 714/2009 and (EC) No 715/2009 (OJ L 115, 25.4.2013, p. 39).

[47] COM(2021) 8409 final.

If a Member State would aim to grant State aid to the project in question, a notification by a Member State of the planned aid would ideally take place at least at the same time as the submission of the application for recognition under the Chips Act. The pre-notification phase could be used to ensure an alignment of both procedures for the State aid authorisation and the recognition of Integrated Production Facilities and Open EU Foundries. The respective assessments would be carried out in parallel, with coordination between the relevant Commission services regarding the compliance with the criteria for Integrated Production Facilities and Open EU Foundries respectively. The Commission services would aim to prepare simultaneous decisions, the timeframe of which would depend on the duration of the State aid assessment, depending on the merits of each individual case under review.

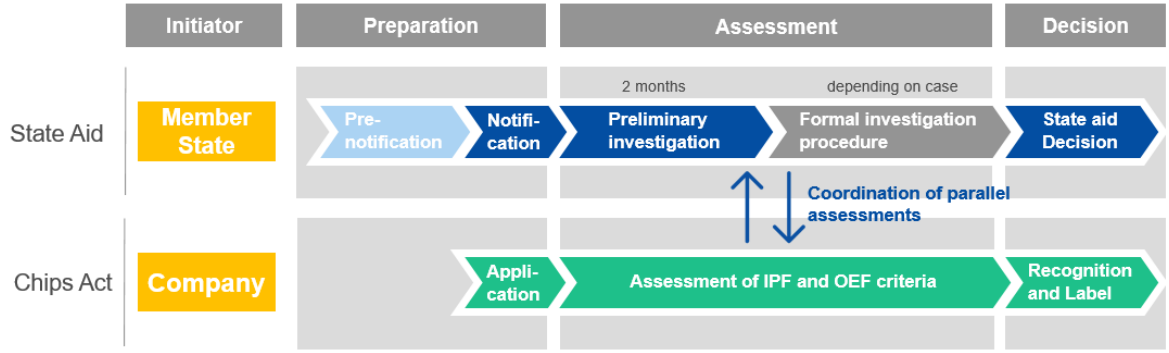


Figure 45. Comparative timelines of procedures of State aid notification and recognition as Integrated Production Facility or Open EU Foundry.

8.2.3 Impact and benefits

Maintaining a competitive semiconductor industry is crucial for the EU economy. Regions with a thriving semiconductor ecosystem derive several benefits such as industrial innovation, export opportunities, highly qualified and stimulating employment and overall economic growth. The examples below are to be read in the context of a need for supported projects to bring positive "pan-European" effects that can be shared widely and without discrimination across the EU economy.

In the global semiconductor industry, the average level of capital expenditures with respect to sales revenues has been consistently above 15%, even rising above 20% in the last few years (26% in 2021). If the average of 15% would be applied to the European industry, it would currently translate into a yearly capacity for capital spending of around EUR 6 billion, with the applicable future growth for the coming years. This gives a dimension of the level of investments that is reasonable to expect in the EU until the end of the decade.

The issue is that in the past 10-15 years, the level of CapEx investments of EU companies has remained stable, whereas that has steeply increased in other regions, with worldwide capital expenditures tripling in the last 10 years. The average investment share of EU companies has therefore gone down below 4% of global capital spending[48], as shown in figure 43.

Investments in production facilities in Europe in the past two decades was rather limited, as a consequence EU's share of worldwide capacity decreased from 11.7% in 2005 down **to 7.2%** in 2020 (see figure 19), with little presence in the more advanced digital nodes. The Chips Act could stimulate

[48] Source IC insights, McClean report 2022.

the potential for capital investment in the EU, contributing to building up the capacity necessary to respond to the growing demands of user industries.

Timely investments in manufacturing capacity are critical for the EU to successfully reach its ambitions. Initial investments in the 2024-25 period[49] would help to consolidate the position of the EU and a second wave of investments in 2026 to 2030 would drive an increasing market share towards the 20% objective by 2030.

The presence of semiconductor fabs in a region attracts the collaboration of many types of companies active in different fields across the entire value chain, such as design, testing, packaging, research and technology services, equipment and raw material, that generate additional innovation and economic value. The creation of Open EU Foundries should be instrumental in allowing to maintain and grow EU's semiconductor ecosystem overall, building on existing strengths outlined in section 3.3.

In order to master the complexity of such advanced technologies, close interactions among the different actors are required, therefore physical proximity is an important advantage. A well-known example is in the region that takes its name from the semiconductors industry that was born there, Silicon Valley, but that is not the only one. In Taiwan, for instance, in 1989 the government decided to promote the local development of the semiconductor industry and invested in a new Joint Venture with the Dutch chipmaker Philips, named Taiwan Semiconductor Manufacturing Company (TSMC), and that was the start of a flourishing local industry. Today in Taiwan, next to TSMC, which is a key player in the foundry market with over 56% share of global sales, there is UMC, the 3rd largest foundry, ASE, the global leader in back-end assembly, package and testing with 57% market share, Mediatek and Novatek, two of the world's largest fabless companies, as well as leading research and technology institutes such as ITRI and TSRI. This ecosystem, built around the first open foundry, makes Taiwan's industry the 2nd largest in the world, with an output of over EUR 100 billion per year, and an essential player in the global value chain.

In the EU, publicly funded fab projects have shown important positive effects as well. To take the most recent case, the new semiconductor fab of Bosch, which recently opened in Dresden (DE) following the fundamentally innovative know-how generated thanks to the support of the German government in the context of the first IPCEI on Microelectronics, has already demonstrated positive spill-over effects, connecting with the EU's semiconductor ecosystem (see box below).

[49] See for example the recent announcements of investments by Intel, as well as the collaboration between STMicroeletronics, GlobalFoundries, Soitec and CEA (https://www.cea.fr/english/Pages/News/roadmap-fdsoi-stm-soitec-gf-cea.aspx).

Example: BOSCH's new fab in Dresden, Germany

The IPCEI project laying out foundations for a new semiconductor site in Germany is still running, and so far it has produced the following spill-over results:

- Triggered private investments of approx. 1 billion EUR in microelectronics in the EU
  - Construction of facilities over 70,000 m^2 of floor space
  - AIoT facility in the EU: Fully connected and self-optimising, involving advanced automation technologies from several partners
  - Strong focus on demands from European users with leading-edge automotive technology capabilities
- Pushing the limits in know-how, skills and cutting-edge innovation
  - Creation of highly qualified jobs for up to 700 associates
  - Strong collaboration with European semiconductor ecosystem to foster skills in AI, Big-Data, technology development, process- and equipment engineering
- Cooperation with several European universities on education and training
  - More than 140 sensor training kits provided to students in 7 Member States; Mentoring of over 12 doctorate degree studies in several Member States
  - Development of sensor use cases for future mobility, smart agriculture, climate monitoring, resource efficient manufacturing logistics, smart health monitoring, and still many more to come
- Talent management and development
  - International student competition events for future mobility, IoT and sensor hackathon
  - Open Big Data Summer School with focus on MEMS sensors in Budapest
- Collaboration with new and existing partners in publicly funded projects
  - Partnering to continue IPCEI related technology development in several ECSEL/KDT projects
  - Partnering in several national and European R&I projects on trusted electronics
- MEMS Foundry Service
  - Bosch to open its technology capability to external partners
  - First projects started with two SMEs on LiDAR sensors and timing devices; one project with a large enterprise on MEMS substrate material
  - Active public offering via conferences, journals and internet
- Multi-design wafer runs
  - Set-up process to allow several MEMS designs to be integrated in one wafer run
  - Cost-efficient concept for universities and RTO's including student training; cooperation with universities in EU (e.g. Minho, PT)

Semiconductor fabs need to innovate continuously, and they are catalysts for further innovation across the entire technology ecosystem. They spur important investments in research and innovation. The semiconductor industry indeed is one of the most research-intensive sectors overall, spending 15-20% of revenues in R&D, and there is an important return on the investments. Public support for such R&D activities can well be justified. This is why specific State aid Guidelines exist for Research, Development and Innovation in Europe. According to a study from SIA, the US federal investments in semiconductor R&D have triggered an increase in the national gross domestic product that is 16 times higher[50].

Investments in such ecosystems generate increased economic activities and incentivize **larger investments from the private sector in many downstream industries,** with a far greater financial impact, since semiconductor products are key enablers of applications in all sectors of the European

[50] Study from the Semiconductors Industry Association https://www.semiconductors.org/wp-content/uploads/2020/06/SIA_Sparking-Innovation2020.pdf.

economy and for the benefit of society. In addition to the direct impact of the activities of the semiconductor industry, we must consider the indirect impact of the upstream and downstream value chains. Beyond the turnover generated by chip manufacturers active in the EU, according to data from *DECISION*[51], in terms of value generated in the downstream electronics value chain, there is a multiplying factor of three times at the level of electronic assemblies, and eight times at the level of electronic systems.

Local semiconductor ecosystems can also generate **important employment opportunities, attracting and retaining talent and raising the skill levels.** According to Eurostat, in 2018 the EU 27 accounted for 219 000 employees in the manufacturing of electronic components, with an annual growth rate of 3% over the 2012-2018 period. *DECISION*[52] estimates that the microelectronics sector in the EU, including design and production of components, materials and equipment, is directly responsible for 455 000 high-skilled jobs. Moreover, as an enabling sector for the entire electronics value chain, from materials to systems, it accounts for 2.6 million jobs in total (see table 2). The demand for new skills is also increasing. The expected investments resulting from the establishment of the framework proposed under the second pillar of the Chips Act therefore could contribute to the creation of thousands of additional jobs in this and related sectors.

Sector	*Companies*	*Employees*
Materials & equipment	24	165 000
Electronic components	47	290 000
Electronic assembly	126	765 000
Electronic systems	290	1 350 000
TOTAL	487	2 570 000

Table 2. Employment in microelectronics sector Europe in 2018 (Source: DECISION[89])

In terms of induced employment, according to SIA and Oxford Economics[53], **for each worker employed by the semiconductor industry, an additional 5.7 jobs are supported in other sectors of the economy.** Therefore, the semiconductor industry has an employment multiplier of 6.7, one of the highest of any industry. In its recent announcement of investments in Europe, Intel specified that the new fab they plan to set up in Germany should employ around 3 000 highly qualified professionals, and that it would support 14 000 to 17 000 additional jobs in the broader economy, with an employment multiplier of 6.2.

Furthermore, advances in production processes often include **improvements on energy-efficiency and environmental impact of factories** and are consistent with the European Climate Law[54]**.** Supporting

[51] Study on the Electronics Ecosystem: Overview, Developments and Europe's Position in the World (EU 2018-19)
[52] Analysis of skills needs and occupational profiles for microelectronics (METIS programme 2020-21)
[53] Study from Oxford Economics and Semiconductors Industry Association: https://www.semiconductors.org/wp-content/uploads/2021/05/SIA-Impact_May2021-FINAL-May-19-2021_2.pdf.
[54] Regulation (EU) 2021/1119 establishing the framework for achieving climate neutrality. 30/06/2021

the production of **more energy-efficient and environmentally friendly components throughout their whole life cycle** (i.e. production, operation, end-of-life) based on innovative approaches (e.g. the development of more efficient manufacturing technologies with a reduced use of energy and materials, the design of semiconductors able to operate with lower levels of energy) would also help limiting the growing impact of the sector on climate and environment. Thanks to technology advances, manufacturing fabs with advanced lithography equipment can produce chips at smaller nodes that are more energy efficient. Processor chips tend to reduce power consumption by nearly two-thirds every two years. Furthermore, power electronics chips, particularly the new generation based on Silicon Carbide, are the key enablers of electric mobility and of all power conversion and transmission systems of renewable energy sources. Therefore, the chips produced by these new facilities can greatly contribute to the achievement of the objectives of the EU Green Deal.

8.3 Pillar 3. Monitoring and Crisis response

8.3.1 Urgency for the EU to start monitoring the semiconductor supply chain

Chips are ensuring essential functions in nearly every technology product today (see Chapter 1) and any shortage in their supply (such as the ones experienced over the past two years – see Chapter 2) can potentially affect many economic and social activities, including the most essential ones.

The supply of semiconductor devices is essential for some industries that are critical for the functioning of the EU's economy and society. This includes sectors such as energy, transport, finance, health, utilities, defence, and public safety and security. Among these critical sectors, several depend on specific types of chips that are difficult to substitute as they are designed in compliance with certain safety requirements (see, for example, section 2.4.2). Furthermore, critical sectors that typically purchase smaller quantities are struggling to buy semiconductors on the market in crisis situations in which foundries give preference to high volume demand (see, for example, section 2.4.3). This leaves critical sectors particularly vulnerable in shortages and hence, exposed to production disruptions. Other sectors of significant economic importance in the EU, such as automotive and industrial automation, also heavily depend on the supply of chips for their production.

An important lesson from the current shortage is that the **lack of availability of relevant detailed information** makes it difficult to establish a precise assessment of risks related to potential disruptions of supplies. There is a need for more data to be shared about production capacities, choke points, and needs of companies in critical sectors. Overall, similarly to what was already done in the United States[55], the EU needs to develop an in-depth understanding and increased transparency of global semiconductor supply chains. While the Commission is already working together with the Member States to understand fully the impact of the current supply disruptions on Europe's industrial ecosystems,[56] this emphasises the need for a permanent mechanism allowing continuous, effective and coordinated information gathering and exchange at EU level on a regular basis.

The current shortage has demonstrated the **need for improved tools to address emergency situations.** Firstly, there is no instrument at EU level to allow for ad hoc gathering of information that enables decision-makers to adapt their policy responses to the shift in conditions and shortages. Secondly, in view of the demonstrated vulnerability of critical sectors in a semiconductor shortage, there is a lack of solutions to ensure the appropriate allocation of products available to priority areas when necessary and avoiding complete disruptions for critical sectors.

In this context, **actions have been initiated at national level** in order to better anticipate and mitigate the effects of shortages[57]. Other Member States might decide as well to tackle the semiconductor shortages by means of national measures, in particular due to the significant impact of shortages on other (strategic) markets and economic sectors. Given the intrinsic cross-border nature of the concerned markets, the semiconductor crisis would be further aggravated with the adoption of new initiatives in

[55] The US Department of Commerce has conducted a survey and assessment of the state-of-play of its semiconductor industry. The results have been presented on 25 January 2022. (Source)

[56] In early 2022, the European Commission has carried out a targeted stakeholder survey ('EU Chips Survey') (https://ec.europa.eu/growth/news/stakeholder-survey-european-chip-demand-2022-02-16_en). The European Commission will publish an overview of the aggregated results of the EU Chips Survey as part of a Factual Summary Report during Q3 of 2022. These will help to provide crucial information on sources and impacts of the supply survey.

[57] Spain announced its intention to reform its National Security Law (*Ley de Seguridad Nacional*) and to cover, amongst other, semiconductors therewith. The envisaged law would allow to establish a list of critical products, monitor the production capacities, create a strategic reserve thereof, and introduce obligations for producers to ensure security of supply and possibly address priority needs in case of crisis situation.

some Member States, while other Member States that are equally impacted by the crisis might take no action. Without action at EU level, the resulting regulatory fragmentation would seriously undermine the functioning of the single market.

The Commission has therefore proposed in the Chips Act to **foster coordination at Union level to better anticipate and react to potential shortages of semiconductors.** Beyond the above-mentioned risk for the proper functioning of the single market, action at EU level would allow to address the issue in a more efficient way, notably in view of the structure of the semiconductors value chain, which features a high-level of concentration in some segments (see section 1.2.3).

Such cooperation between Member States and the European Commission will strengthen the EU's and Member States' abilities to react to crises related to disruptions of the semiconductor supply chain. It will also optimize the allocation of resources and increase the efficiency of relevant measures.

8.3.2 Explaining further the pillar 3 approach

The Chips Act proposes a mechanism for coordinated monitoring of the semiconductor value chain and crisis response to shortages of semiconductors. This would include a **monitoring scheme** under which the national competent authorities of Member States carry out regular observatory tasks and provide for a mechanism to receive updates on demand fluctuations from the industry. The information would be discussed in the European Semiconductor Board. Discussions would include an **early warning and crisis mechanism**, whereby Member States alert the Commission of potential shortages. The Commission would assess the situation and, if necessary, activate the semiconductor crisis stage via an implementing act. After such a crisis has been triggered, the Commission may use a set of exceptional crisis response measures from a **crisis toolbox**.

Monitoring: To address the current **lack of availability of relevant detailed information**, the Chips Act proposes a mechanism for monitoring of the semiconductor value chain. Member States should monitor certain **early warning indicators** for a potential shortage. The early warning indicators are to be developed by the Commission in the frame of a risk assessment of the semiconductor supply chain, based on information collected collaboratively with the Member States. The Chips Act gives an indicative list of what these indicators could be.[58] Lead-time for certain chip types is one of the most important indicators, but also price changes, for both output and input, abnormal fluctuations in demand, and logistics data. Knowledge of events disrupting the supply chain, such as military conflicts and natural disasters, will also play an important role. Furthermore, Member States should monitor the availability and integrity of the products and services of **key market actors**. Key market actors are important players in the semiconductor industry, essential to the functioning of the semiconductor supply chain in the EU. Business closures, delocalisations or acquisitions of these key market actors could have a disruptive effect to the semiconductor ecosystem in the EU. This should be taken into particular consideration, for instance with regard to foreign direct investment[59].

The proposed monitoring mechanism would include information exchange with user industries. The practical implementation could, for example, build on individual industry initiatives, which strive to anticipate the total effective demand for critical semiconductors such as microcontrollers and analogue

[58] Recital 37: Such indicators could include the availability of raw materials, intermediate products and human capital needed for manufacturing semiconductors, or appropriate manufacturing equipment, the forecasted demand for semiconductors on the Union and global markets, price surges exceeding normal price fluctuation, the effect of accidents, attacks, natural disasters or other serious events, the effect of trade policies, tariffs, export restrictions, trade barriers and other trade related measures, and the effect of business closures, delocalisations or acquisitions of key market actors.

[59] See for example: The Weak Links in China's Drive for Semiconductors, institute Montaigne, January 2021, (Table 6).

chips. Such estimates can be a major challenge, as customers tend to overstate demands especially in times of shortages. Strong fluctuations in prices and inventory levels and long lead times are the regular consequence (bullwhip effect). It is in the interest of industry to moderate such fluctuations. Yet the industry initiatives are not sufficient as they look only at individual supply chains and do not cover all relevant end user industries. In the context of the Chips Act, the total effective demand per chip family could be recorded by aggregating company individual demands and then used to pre-empt shortages.

Pilots have been established in a series of publicly funded projects at EU and national level to create a trusted platform for demand forecast[60]. Such a platform allows chip producers and chip clients to declare chip-specific capacities and demands in an anonymised way and extracts with computational methods the actual demand. The data structures encompass entire semiconductor supply chains from the material suppliers up to the industrial end users of chips. As the platform uses semantic web methods, it is by construction scalable to very large user groups. This work has been in the research phase so far and, if implemented in the framework of the Chips Act, could be validated by industrial users and public authorities to capture early warning indicators for critical markets.

Early warning and crisis mechanism: To address the need for enhanced **coordination at European level to better react to potential shortages of semiconductors,** the Chips Act proposes a mechanism whereby the Commission would be obliged to convene an extraordinary Board meeting when it becomes aware of potential crisis – through an alert by Member State(s) or through other sources, including international partners. In addition, taking account of the global nature of the semiconductor value chain and the importance of international cooperation, the Commission would enter into consultation or cooperation with relevant third countries with a view to seeking cooperative solutions[61]. In the extraordinary Board meeting, the Board will assess together with the Commission whether it is warranted to activate the crisis stage. Furthermore, this extraordinary Board meeting would give rise to the opportunity for Member States to discuss with each other if it would be useful to start joint procurement of certain products, which would be carried out under the framework of Directive 2014/24/EU of the European Parliament and of the Council.[62]

The assessment to trigger a crisis would follow a two-step approach: First, there must be serious disruptions in the supply of semiconductors leading to significant shortages in the EU. Second, these shortages must either entail significant delays or negative effects on one or more important economic sectors, or prevent the supply, repair and maintenance of essential products used by critical sectors.

Emergency Toolbox: When the crisis stage is activated, the Commission would exceptionally be enabled to take certain emergency measures set out in the Regulation. The deployment of each measure would take place in dialogue with the European Semiconductor Board and would be limited to where necessary, appropriate and proportionate in accordance with the EU's international obligations. Out of the toolbox, several tools would be limited in use to the benefit of **critical sectors**. The definition of critical sectors in the Chips Act builds on EU acquis by referring to the sectors listed in the annex to the Commission proposal for a Directive of the European Parliament and of the Council on the resilience of critical entities[63]. Additionally, the defence sector and other activities that are relevant for public

[60] EU project, SAFE-DEED | Safe Deed; ECSEL project Productive 4.0 - A European co-funded innovation and lighthouse project on Digital Industry (productive40.eu); German research project Gaia-X: A Federated Secure Data Infrastructure

[61] International cooperation initiatives include EU-US Trade and Technology Council (TTC), and Digital Policy and Industrial Dialogues with South Korea, Japan, Singapore and Taiwan.

[62] Directive 2014/24/EU of the European Parliament and of the Council of 26 February 2014 on public procurement and repealing Directive 2004/18/EC (OJ L 94, 28.3.2014, p. 65).

[63] COM(2020) 829. 16.12.2020.

safety and security are considered critical sectors for the purpose of the Chips Act. The Commission may further limit the scope of these measures to only some critical sectors.

The Emergency Toolbox will consist of several tools:

- **Information Requests.** To increase the understanding of the supply chain disruptions and enable decision-making in response to a crisis, the Chips Act proposes to empower the Commission to launch mandatory information requests about production capabilities and capacities, current primary disruptions and other existing data necessary to assess the nature of the crisis or to identify and assess potential mitigation or emergency measures to put in place. These would address representative organisations and, if necessary, individual companies operating along the semiconductor supply chain. These ad hoc information requests in a crisis would be complementary to the regular monitoring activities proposed in Article 15, in that the response to these requests would be obligatory and enforceable, with the objective to ensure rapid and efficient access to information necessary in the particular situation and be able to rapidly adapt policy decisions.
- **Priority Rated Orders.** To address the abovementioned lack of instruments to ensure allocation of resources in the EU in a shortage to particularly vulnerable critical sectors, the Chips Act proposes a priority rating obligation for certain companies operating along the semiconductor supply chain. The priority rating obligation entails the enforceable obligation to accept and prioritise an order of crisis-relevant products. This obligation would be enacted through a Commission decision addressed to the individual company, following a case-by-case assessment and only where necessary and proportionate, having regard for the legitimate aims of the undertaking and the cost and effort required for any change in production sequence. The Commission decision would specify the product, quantity and time limit. Any order would be placed at fair and reasonable prices. This obligation is limited in scope. Under Article 21, Integrated Production Facilities and Open EU Foundries, as well as semiconductor undertakings which have accepted such possibility in the context of receiving public support, could receive a priority rated order. This would be possible where necessary and proportionate to ensure the operation of all or certain critical sectors.

  Exceptionally, the scope may be extended to other companies operating along the semiconductor supply chain in the EU, if such a company is subject to a third-country priority rated order measures, and compliance with this obligation could significantly impact the operation of certain critical sectors. For this purpose, any company operating along the semiconductor supply chain in the EU would be obliged to inform the Commission when they are subject to a third-country priority rated order measure.

  The Chips Act provides safeguards for companies. Companies would have a right to redress; they may request the Commission to review the priority rated order, if they are unable to perform the order, or because fulfilling the order would pose an unreasonable burden and particular hardship. Companies which fulfil a priority rated order would in turn receive a liability protection for any breach of contractual obligations required to comply with such order (Article 21 paragraph 6).

  Similar tools are in use in other jurisdictions, including the USA: Priority rated orders are an instrument used for the purpose of national defence provided for under Section 4511, Title I (Prioritization and Allocation), of the US Defense Production Act. The Department of Defense (DoD) is the most frequent user of both Title I and Title III authority. It prioritizes about 300

000 orders each year under Title I for the purpose of national defence.[64] The DoD has primarily used Title III to mitigate critical shortfalls in domestic defence industries.[65] Notably, it has invoked Title III in December 2020 to sustain and strengthen industrial capabilities and defence-critical workforce in recovery of the pandemic.[66]

- **Common Purchasing**. As an additional instrument to ensure allocation of resources to priority areas, the Chips Act proposes a framework for common purchasing of crisis-relevant products. Against the background that certain critical sectors have experienced difficulties to purchase as foundries give priority to high volume demand (see, for example, section 2.4.3), common purchasing would allow to pool the negotiating leverage across the EU. Any use of this instrument would be on initiative of two or more Member States, with whom the responsibility for deployment or re-sale of the procured products would lie. The Commission would act as a central purchasing body and procure on behalf of the participating Member States. The participating Member States and the Commission would stipulate a framework agreement to lay down the specific conditions and procedure for the individual activation of this measure. The proposed centralised approach provides greater negotiating leverage, allowing the Commission to pool demand across the EU and offer greater procurement power for the benefit of critical sectors. [67]

- **Export Authorisations.** Export authorisations can be an effective instrument to increase the knowledge and transparency of supply chains. [68] Any such measure would be introduced under the Framework of Regulation (EU) 2015/479 on common rules for exports.[69] When the crisis stage is activated, the European Semiconductor Board would assess the expected impact of the possible imposition of such measures and provide a non-binding opinion to inform the Commission's assessment under the EU framework of common rules for export. The involvement of the European Semiconductor Board to provide a non-binding opinion allows the Commission to benefit from the expertise of the Board in this context.

Safeguards for security of supply: The Chips Act proposes additional safeguards for the security of supply. In the frame of receiving the label, Integrated Production Facilities and Open EU Foundries commit to inform the Commission about third-country public service obligations to which they are

[64] The Defense Production Act Committee Report to Congress 2019, (Source, p. 8).
[65] Usage of the Defense Production Act throughout history and to combat COVID-19 | Yale School of Management
[66] DOD Announces $74.9 Million in Defense Production Act Title III COVID-19 Actions (Press Release)
[67] Previously used similar tools: The Joint Procurement Agreement (JPA) enables the Commission to organise procurement of medical supplies on behalf of participating Member States. 12 procedures have been launched since 2020, allowing countries to order essential medical supplies for nearly €13 billion. The JPA is based on Art. 168(2) TFEU (support to Member States' cooperation in public health).
The Commission established a centralised approach to procuring COVID-19 vaccines on behalf of Member States, following an agreement between the Commission and Member States based on Council Regulation (EU) 2016/369 (ESI Regulation). The Commission also financed a part of the upfront costs from the €2.7 billion Emergency Support Instrument.
[68] Regulation (EU) 2015/479 of the European Parliament and of the Council on common rules for exports was used for an export authorisation scheme for COVID-19 vaccines, which was in place from 30 January until 31 December 2021. Introducing authorisations for exports of vaccines produced in the Union has helped to improve the transparency of vaccines production, deliveries and supply chains, and to secure deliveries to Europeans in line with companies' contractual obligations.
[69] Under this framework, the Commission is empowered to adopt an export authorisation scheme of six weeks through an implementing act in accordance with the examination procedure, or exceptionally the urgency procedure, in order to prevent or remedy a critical situation caused by the shortage of an essential product (Article 5). Furthermore, the Commission may for the same purpose adopt additional appropriate measures through an implementing act in accordance with the examination procedure (Article 6).

subject (Article 10(2)(c) and Article 11(2)(c)). Additionally, any company operating in the EU would have to inform the Commission about information requests from third countries related to their activities in the semiconductor sector (Article 20 paragraph 5). The rationale behind these safeguards is to inform the Commission of crisis measures arising from third countries. This allows early notification of a semiconductor shortage that may have arisen in a third country and not yet reached the EU. This information would additionally enable the EU to take measures to ensure security of supply if necessary and proportionate.

8.3.3 Impact and benefits

The impact of the current market disruptions (see section 2.4) has demonstrated the need to equip the EU with appropriate tools to anticipate and mitigate the effects of future shortages. The proposed mechanism for coordinated monitoring and crisis response addresses directly the shortcomings identified during the current shortage (see section 8.3.1), notably the lack of structured cooperation between decision-makers and lack of instruments for coordinated crisis response at EU level. It is expected that the proposed mechanism would enable regular coordination and information exchange, allowing to anticipate shortages and for a quicker and more efficient reaction to such, as well as an appropriate allocation of available products in case of severe shortages, with the objective to limit the consequences of shortages on critical sectors.

The proposed monitoring and crisis response mechanism follows a balanced approach *in that it introduces crisis response measures* ***only where these are necessary, appropriate and proportionate*** *in order to ensure supply to critical sectors and* ***in close dialogue with Member States and experts*** *through the European Semiconductor Board.*

The chosen approach does not foresee activities with marginal burden for national authorities and companies under regular operation, while effectively and efficiently enabling anticipation of shortages through an early warning system that foresees action only in the case of indicators of a potential disruption of supply of semiconductors. Any crisis response measure could be enacted only after activation of the crisis stage through an implementing act, allowing for full scrutiny by the Member States in the frame of comitology. For each crisis measure, appropriate safeguards ensure that any potentially burdensome action is taken only after careful evaluation whether this would be necessary, appropriate and proportionate, in close dialogue with Member States and experts through the European Semiconductor Board.

During regular operation of the monitoring and crisis response mechanism, expected activities from national authorities or business would relate to the collection and sharing of information necessary to put in place regular monitoring and early warning. National authorities may incur administrative burden with regard to retrieving necessary data for these monitoring activities and putting in place solutions for secure exchange of such data with private entities, while it is expected that they could benefit from standardised solutions provided for in the European Semiconductor Board. Businesses responding to such requests would incur costs for the technical solutions to make the data available (see section 11).

The implementation of the proposed crisis measures may entail some direct and indirect impact on businesses and other private entities, which would be limited to exceptional situations and be carefully taken into account in each case to ensure they comply with the principle of proportionality. If enacted, the proposed mandatory information requests may incur costs for the technical solutions to make data available (see section 11). This impact would be proportional in light of the expected benefit as the information gathering would enable decision-makers to attain an in-depth understanding of the causes for disruption and to identify mitigating action. If enacted, the proposed priority rated orders are expected to directly incur cost for concerned businesses, in particular for the change in production sequence. Indirectly, customers of the concerned companies may incur costs due to delay or cancellation of their previously placed orders. To ensure this measure remains proportional, **the scope of priority rated orders would be focussed on companies that have likely benefitted from significant public support.** Furthermore, there is no equally effective tool to ensure that available resources are preferentially utilised for products supplied to critical sectors. Common purchasing may imply impact on competitors of the awarded contracting parties as well as on trade. To ensure that such a measure remains proportional, such activity would be subject to the application of the procurement rules of the Financial Regulation[70], which ensure transparent and open procedures. To focus this measure further, common purchasing would be deployed only to the benefit of critical sectors.

The proposed monitoring and crisis response mechanism is expected to reinforce the freedom to conduct a business provided for under Article 16 of the Charter of Fundamental Rights of the European Union (the 'Charter'), by strengthening the resilience to disruptions of the entire semiconductor ecosystem. Nevertheless, some crisis response measures may temporarily limit the freedom to conduct a business and the freedom of contract, provided for under Article 16 of the Charter, and the right to property, provided for under Article 17 of the Charter. Any limitation of these rights would, in accordance with Article 52(1) of the Charter, be provided for by the law, respect the essence of these rights and freedoms, and comply with the principle of proportionality.[71]

[70] Regulation (EU, Euratom) 2018/1046 of the European Parliament and of the Council of 18 July 2018 on the financial rules applicable to the general budget of the Union, amending Regulations (EU) No 1296/2013, (EU) No 1301/2013, (EU) No 1303/2013, (EU) No 1304/2013, (EU) No 1309/2013, (EU) No 1316/2013, (EU) No 223/2014, (EU) No 283/2014, and Decision No 541/2014/EU and repealing Regulation (EU, Euratom) No 966/2012.

[71] See for a detailed analysis of impact on fundamental rights: COM(2022) 46 final, p. 14, 15.

9. Coordination and Governance of the Chips Act

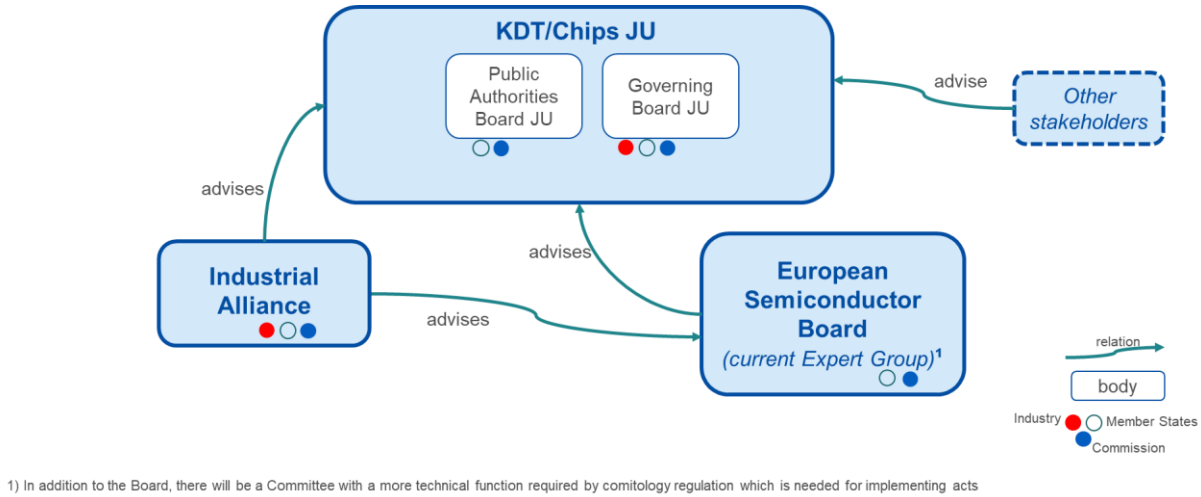


Figure 46. Overview of the proposed coordination and governance structure

The proposed **Chips Act** of 8 February 2022 includes the European Semiconductor Board as the overarching governance structure for the three pillars of activity. In parallel, the proposed amendment to the SBA ('SBA amendment') adapts the functioning of the renamed Chips Joint Undertaking to ensure a proper coordination between the Joint Undertaking (and its different bodies) and the European Semiconductor Board. At the same time, both the Chips Act and the SBA amendment include references to the Industrial Alliance on Processors and Semiconductor Technologies (the 'Alliance'): in the context of the Chips Act, the Commission may invite organisations representing the interests of the semiconductor industry to participate in the European Semiconductor Board in an advisory function or as observers, including, for example, members of the Alliance. In the context of the SBA amendment, it is proposed that the input from stakeholders, such as, but not limited to, the Alliance may be taken into account during the process for shaping the Joint Undertaking's work programmes.

The **European Semiconductor Board** set up by the proposed **Chips Act Regulation** would be a forum that facilitates cooperation and the exchange of information among Member States. Once the Chips Act enters into force, the Board would replace the **Semiconductor Expert Group** referred to in the **Recommendation** published on 8 February 2022. This Expert Group has already been set up to act as platform for coordination between Member States and to provide advice and assistance to the Commission. The Board would consist of representatives from the Member States and is chaired by the Commission. With regards to the Chips Joint Undertaking, the Board would provide advice to the Public Authorities Board (Pillar 1). The Board would also act as an advisory body with respect to Integrated Production Facilities and Open EU Foundries, as well as certification schemes (Pillar 2). Finally, the Board would serve as the coordination mechanism and be consulted in the frame of the monitoring and crisis response measures (Pillar 3). Additionally, it would support the Commission in the area of international cooperation and in the consistent application of the Chips Act.

The **Industrial Alliance on Processors and Semiconductor Technologies**[72] was set up by the Commission in 2021. It is not a body that would be established under the Chips Act or the SBA (amendment). The Chips Act proposes to include it as an advisory body into the governance system, along with other stakeholders. Similarly, the SBA amendment also makes references to roadmaps produced by the Alliance that may serve as advice or guidance to the Joint Undertaking's governing bodies. Dedicated working groups under the Alliance can address specific sectors, such as Defence and Space, to ensure proper representation and facilitate operations.

The SBA amendment would assign the responsibility for the execution of the **Chips for Europe Initiative to the Chips JU** – with the exception of the Chips Fund. This would introduce a structure as depicted below: the Chips JU would implement activities under the original KDT JU (also known as 'non-Initiative' activities) and activities under the Chips for Europe Initiative. The latter activities could be broken down in research & innovation activities and in capacity building activities. The original KDT activities are research & innovation activities. All research & innovation activities will be based on the Strategic Research and Innovation Agenda prepared by the industry associations. Horizon Europe would be the funding source for research & innovation activities, whereas the Digital Europe Programme would fund capacity building activities.

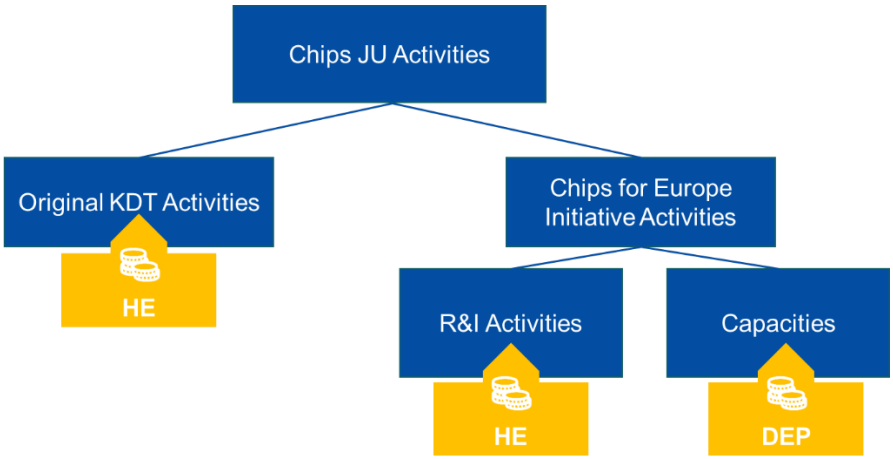


Figure 47. Overview of different activities under the Chips JU

The SBA amendment would introduce slightly changed decision making procedures but would not change the composition of the renamed **Chips Joint Undertaking's** Governing Board (GB) and Public Authorities Board (PAB). It would further extend the role of the PAB, by giving it the task to outline, before the work programme is defined in detail and adopted, the different parts of the work programme as shown above, including their corresponding expenditure estimates. Adoption of the work programmes and project selection would still be done by respectively the Governing Board and the Public Authorities Board, but both would act in different configurations for the Chips for Europe Initiative and the non-Initiative activities.

The **Governing Board**, which would still consist of representatives of participating states, private members, and the Commission, would continue being the main decision-making body of the Joint

[72] The Alliance consists of stakeholders from across the semiconductor value chain, such as RTOs and private companies, and is facilitated by the Commission (formally, the Commission is not a member of the Alliance). The overall objective of the Alliance is to identify current gaps in the production of microchips and the technology developments needed for companies and organisations to thrive. To this end, it will have a General Assembly and specialised working groups.

Undertaking. The GB has the overall responsibility for the strategic orientation and operations of the Joint Undertaking as well as their coherence with relevant Union objectives and policies. In a nutshell, it supervises the implementation of the Joint Undertaking's activities and adopts its work programmes.

The composition of the **PAB** would also remain unchanged; it would still consist of the relevant public authorities of the participating states (Member States and associated countries) and the Commission. The PAB would contribute to the drafting of the strategic research and innovation agenda (SRIA) and would provide input to the draft work programmes, which would later be adopted by the GB. The PAB would also approve the launch of calls for proposals and be responsible for the selection of projects on the basis of the ranking list prepared by the evaluation committee and decide on the allocation of public funding to selected proposals.

Finally, Article 171[73] of the SBA, as currently in force, provides a framework for the monitoring and evaluation of all Joint Undertakings set up in the SBA, including, the KDT Joint Undertaking. This provision will not be changed with the SBA amendment and it will continue applying to the proposed Chips Joint Undertaking. This framework ensures a continuous monitoring of the management and implementation of the activities of the Chips Joint Undertaking, in accordance with its financial rules, in order to ensure the highest impact, scientific excellence and the most effective and efficient use of resources.

Monitoring and reporting will include, amongst other, time-bound indicators for the purpose of reporting on the progress of the Chips Joint Undertaking's activities towards the achievement of its general, specific and operational objectives; information on synergies between the Chips Joint Undertaking's actions and national or regional initiatives and policies; information on quantitative and qualitative leverage effects; and information on measures to attract newcomers, particularly SMEs, higher education institutions and research organisations, and to expand collaborative networks.

To this end, the Commission will carry out an interim and a final evaluation of the Chips Joint Undertaking, which will feed into the Horizon Europe evaluations. These evaluations will examine how the Chips Joint Undertaking fulfils its mission and objectives as well as its European added value, effectiveness, efficiency, including its openness and transparency, the relevance of the activities pursued and their coherence and complementarity with relevant regional, national and Union policies, including synergies with other parts of Horizon Europe. These evaluations will also take into account the views of stakeholders, at both European and national level."

[73] Article 171 (Monitoring and evaluation) of the SBA (Council Regulation (EU) 2021/2085). See SBA link: https://eur-lex.europa.eu/legal-content/EN/TXT/?uri=CELEX:32021R2085

10. Budgetary Aspects

10.1 Investment

The European Chips Act is to be supported with an estimated overall level of policy-driven investment in excess of EUR 43 billion up to 2030[74]. The expectation is that this will attract similar levels of long-term private funding. The overall public investment will include EUR 11 billion for the Chips for Europe Initiative which targets technology leadership in research, design and manufacturing capacities up to 2030[75]. A key aim is to pool investment from the Union, private investors and the Member States to provide the critical mass of funding required. Additionally, underpinning this investment equity support will be provided to start-ups, scale-ups and other companies in the supply chain via a EUR 2 billion 'Chips Fund'. Together these should result in public and private investments exceeding EUR 15 billion.

Furthermore, loans from the EIB for the entire semiconductor ecosystem will be made available. At the Member State level additional support for the Chips for Europe Initiative may also come from national or regional funds and funding targeting microelectronics in recovery and resilience plans. Unused loan capacity under the Recovery and Resilience Facility can also be used by Member States to provide support. This complements activities such as the new IPCEI which will support cross-border innovative projects along the microelectronics value chain, including through the Recovery and Resilience Facility and Structural Funds. Additionally, there will also be support for setting up of large manufacturing facilities. Although the specific amount cannot be announced yet, it is expected that public investments by Member States, coming from Recovery and Resilience Plans, Cohesion Fund plans, national budgets etc. for purposes such as the IPCEI and large manufacturing projects, would total EUR 30 billion.

10.2 Breakdown of Funding Components

The budgetary construction of the Chips Act proposal is described in the **legislative and financial statement** (LFS) accompanying the proposed Chips Act.[76]

The EU budget will support the Chips for Europe Initiative with funding of **up to EUR 3.3 billion**, including EUR 1.65 billion via Horizon Europe and EUR 1.65 billion via the Digital Europe Programme. Out of this total amount, EUR 2.875 billion will be implemented through the Chips JU, EUR 125 million through InvestEU (against which the EIB group is expected to provide additional financing of up to EUR 125 million) and EUR 300 million through the European Innovation Council. This comes in addition to the budget already dedicated to activities in microelectronics planned for 2021-27 to reach almost EUR 5 billion.

- **Horizon Europe**: an amount of up to EUR 1.65 billion will be implemented under HE in favour of the Chips for Europe Initiative, including EUR 300 million under the European Innovation Council (EIC), and 500 million from the current EUR 1.8 billion dedicated to the Key Digital Technologies Joint Undertaking.
- **Digital Europe Programme**: a new Specific Objective 6 is proposed for the purposes of the Chips for Europe Initiative. The Specific Objective 6 covers components a) to e) of Article 5

[74] Public investment and leveraged equity support.
[75] EUR 5.85 billion EU investment + EUR 5.3 billion MS investment.
[76] Financial details on the amendment of Regulation 2021/2085 establishing the Joint Undertakings under Horizon Europe (for the Chips JU) are provided in the Legislative Financial Statement annexed to the Chips Act proposal.

of the Chips Act[77] (see section below). A total of up to **EUR 1.65 billion** will be allocated to this new Specific Objective 6 of the programme, through reallocation from the existing objectives of the DEP, a contribution from the Connecting Europe Facility Programme (CEF)and from the unallocated margin of Heading 1 and decommitments from the HE programme.

In order to compensate for the decommitments of Horizon Europe, the Commission proposes to make available again, for the benefit of the HE programme, a further amount of commitment appropriations over the period 2023-2027, resulting from total or partial non-implementation of projects belonging to that programme or its predecessor. This amount will be in addition to the EUR 500 million (in 2018 prices) already mentioned in the Joint Declaration by the European Parliament, the Council and the Commission on the re-use of decommitted funds in relation to the research programme.

[77] The 5 components are: (a) design capacities for integrated semiconductor technologies; (b) pilot lines for preparing innovative production, and testing and experimentation facilities; (c) advanced technology and engineering capacities for quantum chips; (d) a network of competence centres and skills development; and (e) 'Chips Fund' activities for access to debt financing and equity to start-ups, scale-ups, SMEs and other companies in the semiconductor value chain.

Budget implementation - the Chips Joint Undertaking

The Regulation 2021/2085 establishing the Joint Undertakings under Horizon Europe (Single Basic Act (SBA)) is amended and expanded to allow the Key Digital Technologies Undertaking (KDT JU), renamed as **Chips Joint Undertaking (Chips JU)** to implement most of the increased contribution from HE and contributions from DEP under the Specific Objective 6.

The components under the Chips for Europe Initiative listed in points (a) to (d) of Art. 5 of the Chips Act may be entrusted to the Chips JU and implemented in its work programme[133].

Article 128 of the proposed amendment to the SBA, as regards the Chips JU, indicates that the proposed Union financial contribution '*shall be up to **EUR 4.175 billion***'.

Most of the budget of the Initiative mentioned above (up to **EUR 1.65 billion from HE +** up to **1.65 billion from DEP**) will be channelled via the Chips JU, with the **exception** of:

- **EUR 125 million** of the Digital Europe Programme, which will be implemented under InvestEU, and
- **EUR 300 million** of the European Innovation Council (part of the Horizon Europe programme), which will be implemented by the EIC.

Finally, the budget of the current KDT JU (**EUR 1.3 billion**, given that EUR 500 million of the EUR 1.8 billion currently indicated in the SBA are earmarked for the Chips for Europe Initiative, as indicated above) will continue being part of the budget of the renamed Chips JU.

This leads to the total Union contribution of 'up to **EUR 4.175 billion**', of which EUR 1.525 billion from the Digital Europe Programme and EUR 2.65 billion from Horizon Europe. This leads to the following breakdown (in EUR billion):

	Chips for Europe Initiative	Non-Initiative	Total
Research & Innovation (Horizon Europe)	1.350	1.300	2.650
Capacity building (Digital Europe)	1.525	n.a.	1.525
Total	2.875	1.300	4.175

11. Application of the ‘one in, one out’ approach

The implementation of the Chips Act is expected to create no administrative cost for citizens and only a marginal administrative cost for businesses. The expected administrative cost for businesses relates primarily to the new monitoring and crisis response measures under the Pillar 3 of the Chips Act as outlined in Chapter 4 of the Proposal for a Regulation[78] and in Section 8.3 of this SWD. Pillar 2 “A Framework to ensure Security of Supply”, outlined in Section 8.2 of this SWD, while voluntary in nature, may incur administrative cost for businesses. However, these administrative costs would be non-significant. Pillar 1 “The Chips for Europe Initiative” of the Proposal for a Regulation, as outlined in Section 8.1, puts forward measures of a voluntary nature (e.g. applications for R&I support) and as such does not imply an administrative cost for businesses.

Under Pillar 2, the expected administrative costs would result from participation in the voluntary framework for “Integrated Production Facilities” and “Open EU Foundries”. Businesses would have to provide certain documentation, specified in Article 12, when applying for recognition of their project as either type of facility. However, it is expected that businesses would have this information available, as it is documentation typically required to receive financial support. Additionally, there might be further synergies in procedures if a business also seeks public support. The Commission’s monitoring of businesses recognised as “Integrated Production Facility” or “Open EU Foundry” may incur administrative costs for these businesses. This administrative cost would depend on the frequency and type of documentation required, but would be limited to companies voluntarily participating in the scheme, which in turn receive several benefits (see Section 8.2.2). Therefore, the incurred administrative cost may be considered as non-significant.

Under Pillar 3, a distinction must be made between the nature of the obligations deriving from the regular monitoring activities and the crisis response measures. Under Article 15 of the Proposal for a Regulation, Member States *shall invite* the main users of semiconductors and other relevant stakeholders to provide information regarding significant fluctuations in demand and known disruptions of their supply chain. The provision of such information would be voluntary. The administrative cost for businesses depends on many factors, such as the type of infrastructure needed, the format in which data would be delivered and the level of customisation needed, as well as on the frequency of the invitations for monitoring (monthly, bimonthly, or quarterly). With the information at hand and considering that a limited number of businesses, mostly large companies users and suppliers of chips, would be involved in the process, the administrative cost for providing information is considered marginal.

According to Article 20 of the Proposal for a Regulation, in case of the activation of the crisis stage, the Commission *shall request* representative businesses operating along the semiconductor supply chain to provide information about their production capabilities, production capacities, current primary disruptions and other existing data necessary to assess the nature of the semiconductor crisis or to identify and assess potential mitigation or emergency measures at national or Union level. Addressees of such information requests *shall* supply the requested information. The crisis stage would be activated in exceptional circumstances only, as defined in Article 18. The information that businesses would need to provide in case of a crisis would be of a similar nature and volume to the information that they are already collecting on a regular basis for various business practices, e.g. for ensuring business continuity, and it is expected that businesses can benefit from solutions put in place in the context of the monitoring

[78] COM(2022) 46. Proposal for a Regulation establishing a framework of measures for strengthening Europe's semiconductor ecosystem (Chips Act). 08/02/2022

activities. Hence, the new legal obligation of sharing this information with the Commission in case of a crisis would not imply a significant administrative cost.

The details for implementation of the crisis response measures under Pillar 3 of the Proposal for a Regulation are still under negotiation with the Member States, as well as under consultation with the EU semiconductor industry. Even though at the present moment the administrative cost resulting from these measures is expected to be non-significant, an accurate estimation would only be possible once the discussions on the implementation are complete.

Overall, the Chips Act's new monitoring and crisis response measures are expected to bring important economic and social benefits by preventing and mitigating disruptions in the supply chain, avoiding market shocks and ensuring the availability of chips, especially for critical sectors. These expected benefits would justify the introduction of a marginal administrative cost for businesses.

12. What success looks like

Success will be measured against the achievement of objectives in an efficient and effective manner. The overarching objective of the EU Chips Act is set by the 2030 Digital Compass[79] and establishes that Europe will deliver 20% of semiconductors world production by 2030. The implementation of the Act in three pillars and correspondent initiatives would allow the follow up of specific objectives and the materialisation of the expected benefits and impacts.

The EU Chips Act will be considered successful if a gradual and tangible progress towards the following objectives can factually be confirmed within the time and resources planned:

- Strengthen EU research and technology leadership
- Address the skills shortage, attract new talent and support the emergence of a skilled workforce
- Reinforce the capacity of Europe for innovation in design, wafer manufacturing and packaging
- Establish a framework to increase substantially production capacity by 2030
- Develop an in-depth understanding of global semiconductor supply chains and enable the EU to take appropriate measures when necessary

[79] COM(2021)118. 2030 Digital Compass: the European way for the Digital Decade. 09/03/2021

Glossary

AI - Artificial Intelligence is used to give a computer or a robot controlled by a computer the ability to do tasks that are usually done by humans that require human intelligence or discernment.

ASICs - Application Specific Integrated Circuits are customed designed circuits for specific applications.

Back-end - Back end semiconductor manufacturing refers to the fabrication processes after all of the features/circuits have been created on the wafer

BiCMOS - BiPolar CMOS technology integrates two semiconductor technologies, those of the bipolar junction transistor and the CMOS (complementary metal-oxide-semiconductor) gate, in a single integrated circuit device.

CAD - Computer Aided Design is the use of computers to aid in the creation, modification, analysis, or optimization of a design. This increases the productivity of the designer, improves the quality of design, improves communications through documentation, and creates a database for manufacturing.

CAGR - Compound Annual Growth Rate is the mean annual growth rate of an investment over a specified period of time longer than one year.

CAPEX - Capital Expenditure

CEF - Connecting Europe Facility Programme is a European Union fund that supports infrastructure investments across the union in transport, energy and digital projects aimed at a greater connectivity between EU member states. It is operated through grants, financial guarantees and project bonds.

Chiplet – chiplet-based design is an approach whereby a single chip is broken down into multiple smaller chiplets and then "re-assembled" using advanced packaging solutions.

CMOS - Complementary Metal Oxide Semiconductors consists of a pair of semiconductors connected to a common secondary voltage such that they operate in opposite (complementary) fashion. CMOS is the predominant semiconductor technology.

CPUs – Central Processing Units are used within microprocessors to execute instructions.

CT - Computerised tomography scans use X-rays and a computer to create detailed images of the inside of the body.

DEP – The Digital Europe Programme is an EU programme that supports technological leadership.

DoD - Department of Defense

EAR - Export Administration Rules

ECG - An electrocardiogram is a test used to check the heart's rhythm and electrical activity.

ECIC - European Chips Infrastructure Consortia

ECSEL JU - Electronic Components and Systems for European Leadership Joint Undertaking is an EU driven, public private partnership, funding innovation in electronic components and systems.

EDA - Electronic Design Automation is a set of software tools for designing electronic systems such as integrated circuits and printed circuit boards. The tools work in a design flow that chip designers use to design and analyse entire semiconductor chips.

EDIHs - European Digital Innovation Hubs will function as “one-stop shops” that help companies dynamically respond to the digital challenges and become more competitive.

EIB - European Investment Bank

EMIB - Embedded Multi-Die Interconnect Bridge technology allows the use of silicon from different process nodes in the same package.

EUV - Extreme Ultraviolet Lithography is an optical lithography technology using a range of extreme ultraviolet (EUV) wavelengths to produce a pattern by exposing a reflective photomask to Ultra Violet light which gets reflected onto a substrate covered by photoresist. Chemicals are then used to etch the substrate along with other processes to create the chip die.

EV - Electric Vehicles use battery technology and one or more electric motors for propulsion.

FID - First Industrial Deployment

FOWLP - Fan-Out Wafer Level Packaging is an integrated circuit packaging technology, and an enhancement of standard wafer-level packaging solutions. It provides a smaller package footprint along with improved thermal and electrical performance compared to conventional packages. Additionally, it allows a higher number of contacts without increasing the die size.

FDSOI - Fully Depleted Silicon on Insulator is a planar process technology that delivers the benefits of reduced silicon geometries while simplifying the manufacturing process. FDSOI provides improved performance and low power.

FETs - F*ield-Effect Transistor*s use an electric field to control the flow of current in a semiconductor.

FinFETs - Fin Field-Effect Transistors are a multigate metal oxide semiconductor field effect transistor. They get their name from the fins formed on the silicon surface. FinFETs provide significantly faster switching times and higher current density than other planar CMOS technologies.

FOAK - First-Of-A-Kind (FOAK), to be introduced under the EU's Chips Act, would allow state aid funding to be used for "first-of-a-kind" production sites in Europe, as part of a larger goal of producing 20 percent of the world's semiconductors by 2030.

FPGAs - Field Programmable Gate Arrays provide programmable logic devices that can be programmed by the end user in the field.

FRAND - Fair, Reasonable and Non-Discriminatory

Front-end - the fabrication from a blank wafer to a completed wafer

GaaFET - Gate all around FET transistors use a modified transistor structure where the gate contacts the channel from all sides which enables continued scaling. GAA transistors offer better performance than FinFETs.

GaN - Gallium Nitride (*GaN*) is a material that can be used in the production of *semiconductor* power devices.

GB - Governing Board (ECSEL)

Gbps - Giga bits per second is a data transfer rate equivalent to one billion bits per second.

GDP - Gross Domestic Product

GDPR - General Data Protection Regulation

GHG - Green House Gas

GPUs – Graphics Processing Units are used in graphics rendering and acceleration, for instance in video processing and gaming applications.

Green Deal – The Green Deal, presented in December 2019, has the overarching objective that the EU should become the first climate neutral continent by 2050, resulting in a cleaner environment, more affordable energy, smarter transport, new jobs and an overall better quality of life.

HE - Horizon Europe supports intensive pre-competitive research, and technology development. This includes innovation in the area of materials and semiconductors.

HPC - High Perfomance Computing

IC - Integrated Circuits are a set of electronic circuits on one small flat piece of semiconductor material, usually silicon.

ICT - Information and Communications Technology is defined as a diverse set of technological tools and resources used to transmit, store, create, share or exchange information. Examples are laptops, routers, data servers, etc.

IDMs - Integrated Device Manufacturers are semiconductor companies which design, manufacture, and sell integrated circuit (IC) products.

IoT - The Internet of Things describes physical objects with sensors, processing ability, software, and other technologies that connect and exchange data with other devices and systems over the Internet or other communications networks.

IP - Intellectual Property blocks/cores are reusable units of logic or integrated circuit layout that are used in chip design that are the intellectual property of one party. IP cores can be licensed to another party or owned and used by a single party.

IPCEI - Important Projects of Common European Interest are large scale projects bringing together companies and research centres from different Member States to provide significant benefits to strategic EU goals (competitiveness, sustainable growth, societal challenges, value creation, …). In the semiconductor area there is an IPCEI on Microelectronics.

IPF - Integrated Production Facilities are vertically integrated semiconductor manufacturing facilities, which are involved in the front-end manufacturing as well as in the design of integrated circuits or the provision of back-end services, such as assembly, testing and packaging, or both.

IRDS - International Roadmap for Devices and Semiconductors is a set of predictions about likely developments in electronic devices and systems published by the IEEE.

JPA - Joint Procurement Agreements enable the Commission to organise collective procurement on behalf of participating Member States.

JU - Joint Undertakings complement the existing Horizon Europe framework by addressing global challenges and priorities that require critical mass and long-term vision. Joint undertakings enable the joint investment of tens of billions of euros by public and private actors, at EU and national level.

KDT - Key Digital Technologies

LEDs – Light Emitting Diodes are a semiconductor light source that emit light when current flows through them. Electrons in the semiconductor recombine with electron holes, releasing energy in the form of photons.

LiDAR - Light Detection and Ranging, is a remote sensing method that uses light in the form of a pulsed laser to measure distances.

Mbps - Megabyte per second is a unit of data transfer rate equal to 8,000,000 bits per second or 1,000,000 bytes per second.

MCU - Microprocessor Control Units direct the operation of other units within a processor by providing timing and control signals. It is the function of the microcomputer to execute programs which are stored in memory in the form of instructions and data.

MEMS - Micro-electromechanical Systems is a process technology used to create tiny integrated devices or systems that combine mechanical and electrical components. They are fabricated using integrated circuit (IC) batch processing techniques and can range in size from a few micrometers to millimetres.

ML - Machine Learning is an Artificial Intelligence approach which focuses on the use of data and algorithms to imitate the way that humans learn, gradually improving accuracy. ML algorithms are trained using three prominent methods: supervised learning, unsupervised learning, and reinforcement learning.

MRI - Magnetic resonance imaging is a medical imaging technique that uses a magnetic field to create detailed images of the organs and tissues in your body.

MS - Member States

NDA - Non-Disclosure Agreement is a legally binding contract that establishes a confidential relationship. The party or parties signing the agreement agree that sensitive information they may obtain will not be made available to any others.

Nm - Nanometres are a unit of length in the metric system, equal to one billionth of a metre. One nanometre can be expressed in scientific notation as 1×10^{-9} m, and as 1/1000000000 metres.

OEM - Original Equipment Manufacturers make systems or components that are used in another company's end product. Computer manufacturers, for example, commonly bundle or integrate OEM parts, such as processors and software, into the solutions they sell.

Open EU Foundries are semiconductor manufacturing facilities which dedicate at least a significant extent of their production capacity to produce chips according to the design of other companies, in particular fabless companies.

OSATs - Outsourced Semiconductor Assembly and Test companies provide third-party IC-packaging and test services.

PAB - Public Authorities Board (ECSEL)

PCB - Printed Circuit Boards have a laminated sandwich structure of conductive and insulating layers onto which chips are integrated to create electronic products.

PDK - Process Design Kits provide a set of files which are used within the semiconductor industry to model a fabrication process. The PDK is created by the foundry defining a certain technology variation for their processes. Foundry customers use this information in their design tools to design appropriate integrated circuits.

PPAC-E - Power, Performance, Area, Cost and Environmental impact

QT - Quantum Technologies are a class of technology that works by using the principles of quantum mechanics (the physics of sub-atomic particles), including quantum entanglement and quantum superposition.

RibbonFET is a new transistor architecture based on gate all around transistors, which Intel plans to start producing commercially in 2024.

RF - Radio Frequency is the oscillation rate of an alternating electric current or voltage, or magnetic/electric/electromagnetic field in the frequency range from around 20 kHz to around 300 GHz.

RISC-V - Reduced Instruction Set Computer -V is an open standard instruction set architecture that began in 2010 and is based on established reduced instruction set computer principles. Unlike most other ISA designs, RISC-V is provided under open source licenses that do not require fees to use.

RoHS – The Restriction of Hazardous Substances Directive 2002/95/EC, restricts the use of certain hazardous substances in electrical and electronic equipment.

RTO - Research and Technology Organisations are specialised knowledge organisations dedicated to the development and transfer of science and technology for the benefit of the economy and society.

SaaS - Software as a Service is a software licensing and delivery model in which software is licensed on a subscription basis and is centrally hosted.

SBA - Single Basic Act

SiC - Silicon Carbide offers advantages over silicon when used in semiconductor technology, including a higher critical breakdown field, which means a voltage rating can be maintained while still reducing the thickness of the device and a wider bandgap, which leads to lower leakage current at relatively high temperatures. This is important for power electronics and is likely to have a big impact on areas such as electromobility.

SIMD - Single Input Multiple Data processing can process multiple data values using a single instruction. One instruction can therefore do the work of many which is very powerful for computations in areas such as media data.

SiP - System-in-Package integration integrates a number of integrated circuits in one or more chip carrier packages that may be stacked using package on package. SiPs are commonly used in mobile phones, digital music players, etc.

SME - Small and Medium Enterprises are defined by the EC as having less than 250 staff, a turnover of less than EUR 50 million and a balance sheet of less than EUR 43 million. Within this definition there are also Small and Micro Companies with less staff and turnover.

SoC - System on Chips integrate all or most components of a computer or other electronic system in a single device.

SOI - Silicon On Insulator fabricates silicon semiconductor devices in a layered silicon–insulator–silicon substrate to reduce parasitic capacitance within the device resulting in an improvement in performance.

TFEU - Treaty on the Functioning of the European Union

TPU - Tensor Processing Units are application specific integrated circuits developed by Google specifically as an AI accelerator for neural network implementation in machine learning.

VC - Venture Capital

3D Stacking is a three-dimensional integrated circuit approach where silicon wafers or dies are interconnected vertically by using through-silicon vias (TSVs) or via Cu-Cu connections, so that they behave as a single device. This results in performance improvements at reduced power and smaller footprint than conventional two-dimensional processes.

"III-V materials" refers to compound semiconductor materials combining elements of the group III and V of the periodic table. Gallium-nitride (GaN) and indium-phosphide (InP) are examples of III-V materials.

4G - 4G stands for "fourth generation" and refers to mobile network technology that enables 4G compatible phones to connect to the internet.

5G - 5G stands for "fifth generation" and this network offers low latency, high datarate communications enabling the connection of people, machines, objects, and devices.

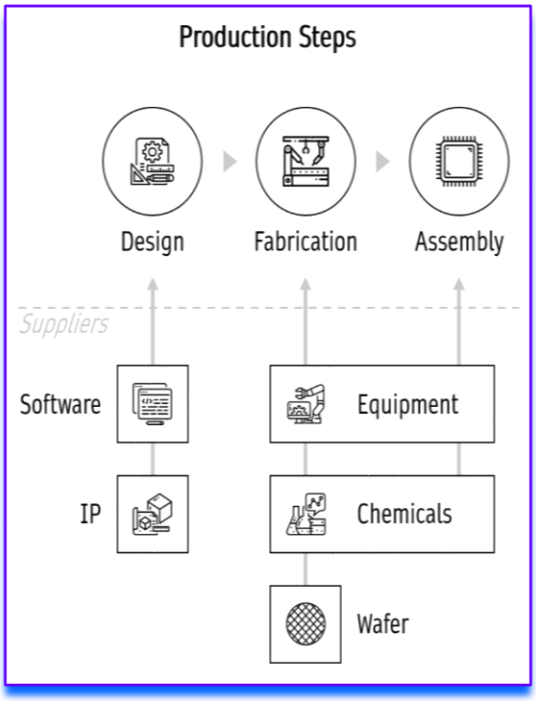
6G - 6G stands for "sixth generation" and is currently under development for wireless communications technologies supporting cellular data networks. This successor to 5G will be significantly faster opening up new concepts such as the "metaverse".

Annex 1. Introduction to Semiconductors

Semiconductors are the material basis for chips[80] embedded in virtually every technology product today. Chips are miniaturised physical devices that can capture, store, process and act on data. They come in many families - some of which are shown in the box below.

Chips are also an enabler for emerging technologies, such as artificial intelligence, quantum computing, and autonomous and electric vehicles. A recent report by the White House[81] refers to semiconductor chips as being "*the 'DNA' of technology*".

The active component of a chip is a transistor - an electronically controlled switch.

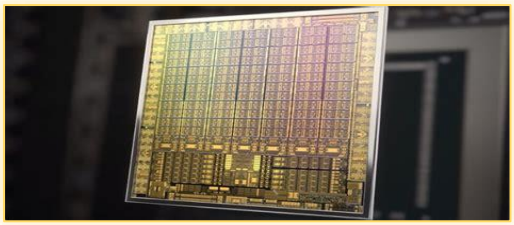


Since the 1960s, the business of chip production has been driven by doubling the amount of transistors in a given area of semiconductor - and hence doubling the computing power without cost - every eighteen months[82].

It is characterised by rapid technological change fuelled by constant research and development (R&D) at all stages of the value chain: from the software and intellectual property[83] that support the process of chip design, to the materials (wafers and chemicals) and equipment that support the processes of fabrication, and subsequent assembly, test and packaging of the chip. Over the last 20 years, the annual R&D expenditure as a percentage of revenues has been consistently between 15 and 20%.

This elaborate process translates to a complex and global supply chain, high capital investment costs with large economies of scale and significant market concentration.

Today, leading-edge fabs are equipped with the most modern process technologies that enable transistors to be printed with a precision of 5 nm[84].



Nvidia's Ampere architecture powers its first 7 nm GPU - it has 28 billion transistors

[80] Often referred to as integrated circuits or ICs.
[81] *Building Resilient Supply Chains, revitalising American Manufacturing, and fostering Broad-based Growth*, June 2021.
[82] Referred to as Moore's Law, dating from 1965 when a chip had just 64 transistors. It's why an iPad today has more processing power than a (refrigerator-sized) Cray supercomputer in 1990. More in Annex 3.
[83] Because of the complexity of designing chips with millions or even billions of transistors, chip designers license intellectual property or IP blocks (essentially basic functional building blocks or architectures).
[84] In semiconductor manufacturing, the process technology (or process node) has traditionally been correlated with the transistor dimension. It is measured in nanometres: 1 nm or 1 nanometre = 1 billionth of a meter. Smaller process nodes produce smaller transistors, which are faster and more power efficient. The state-of-the-art process node is 5 nm today, with 3 nm in pre-production and 2 nm under development. Only TSMC and Samsung, are producing at 5 nm (Intel is struggling with 7 nm).

Chips such as GPUs[85] designed for very compute-intensive applications have around 50 billion transistors. The cost of building a leading-edge fab can be up to EUR 20 billion; designing and developing such a complex chip can be in the range of EUR 1 billion[86].

Given the cost of building a modern fab and developing new process technology, the fab production line needs to be kept full. The volume required for cost-effective manufacturing is so high[87] that very few semiconductor companies can fill their own fab even if they could afford to build it.

This has transformed the business dramatically. Previously dominated by Integrated Device Manufacturers (IDMs) who design their own chips and have their own facilities for fabrication and assembly, today most companies run their businesses based on "fabless" or "fab-lite" models whereby they outsource all or some of their fabrication to foundries[88].

Further, only a small handful of foundries have the financial and commercial muscle to build leading-edge fabs, driven by microprocessors for computers and mobile handsets - high volume businesses that need the highest possible performance and the lowest possible power.

The other part of the foundry business is not focused on the leading edge but on designs for sensors, power management, and so on. For these designs, the state-of-the-art process today is 65 nm and so does not require the most leading-edge fab.

[85] Graphics Processing Units (GPUs) are used to accelerate computing processes, for graphics rendering in gaming and are increasingly important for artificial intelligence due to their capability to process large data volumes with high efficiency. Nvidia developed GPU technology and is currently the market leader.
[86] https://www.extremetech.com/computing/272096-3nm-process-node
[87] At least 50,000 wafers per month for the most modern fabs. Wafers are generally 300mm in diameter. One such wafer would hold 150 (giant) chips of 20x20mm. This would equate to 7.5 million chips per month.
[88] TSMC is the world's largest foundry with revenues of USD 34 billion. Intel, nowadays an IDM, designs and fabricates its own chips, but has recently announced its intention to enter the foundry business.

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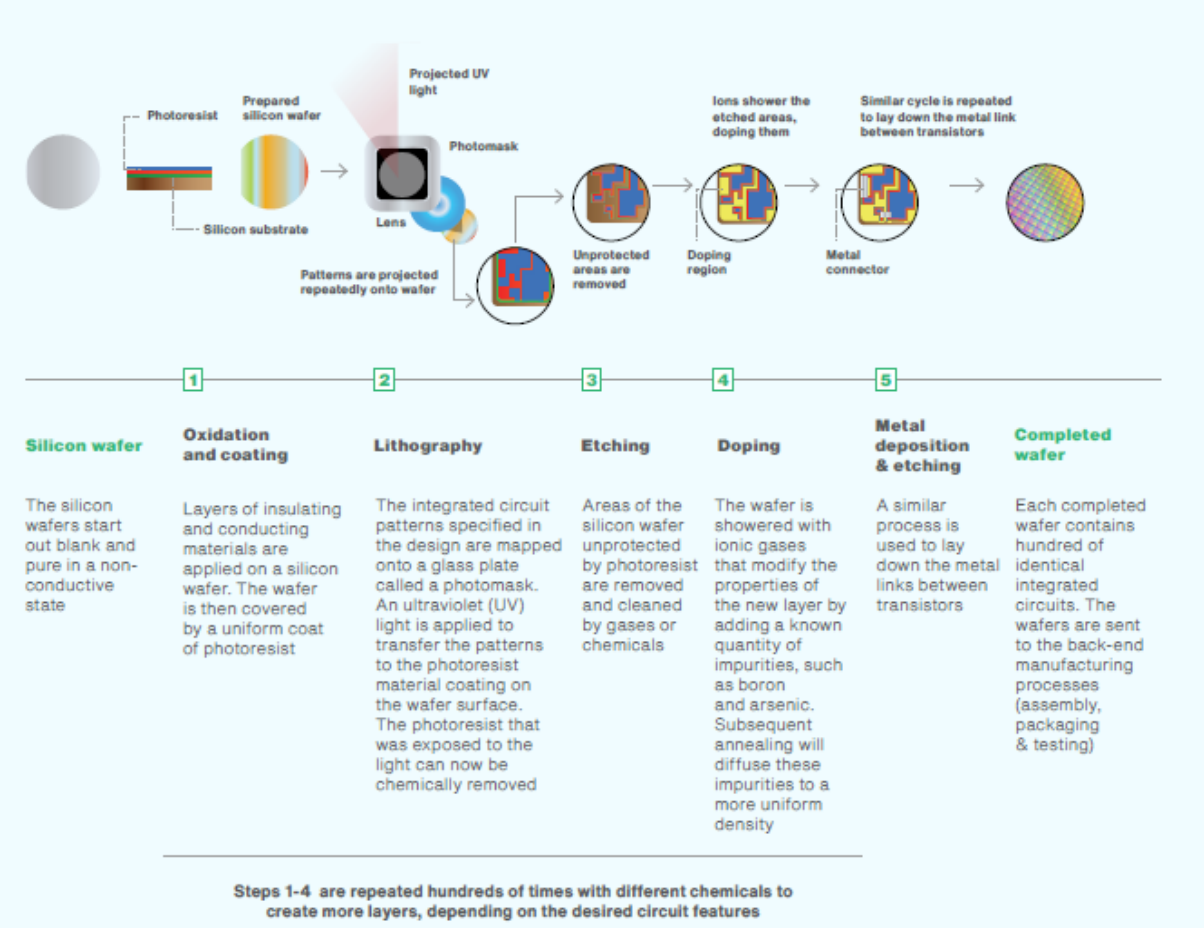
PART 4/4

COMMISSION STAFF WORKING DOCUMENT

A Chips Act for Europe

Annex 2. Semiconductor Manufacturing Steps

The main steps in the chip manufacturing process are set out in the following schematic[1]:



The key feature of the manufacturing process is that all the transistors on all the die[2] on the wafer are created simultaneously, and each layer of metal is created simultaneously across the whole wafer. It is this incredible level of efficiency, making trillions of transistors at once, that has allowed the price of electronic products to fall by around 5% per month, year after year.

It is worth emphasizing that the manufacturing process doesn't depend on what is being manufactured. A computer printer does not need to be reconfigured depending on what you want to print, you just send it different data. In the same way, a semiconductor manufacturing process doesn't depend on what the circuit is going to do.

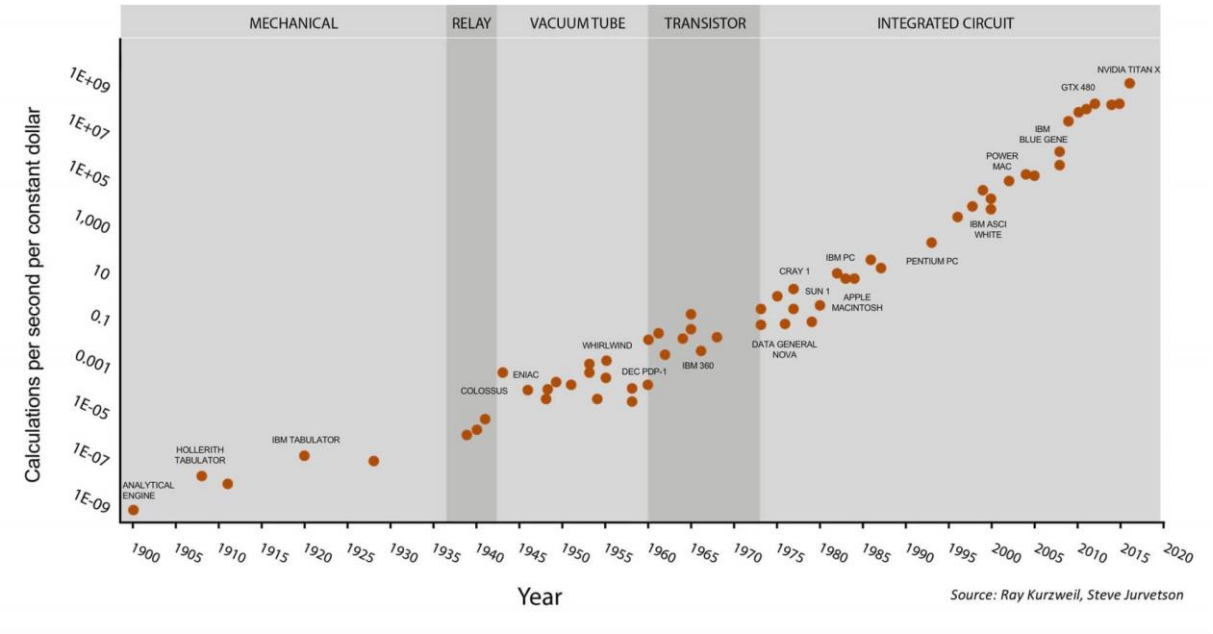
The fab where chips are manufactured are kept very clean - the air may be completely changed every few seconds, as particulate filters in the ceiling blow air down and out through perforations in the floor before being filtered and recirculated. Recently, fabs have found that even that air is not clean enough. A few random particles landing on a die can ruin it. These days, the wafers being processed are contained in even cleaner boxes that attach to each piece of manufacturing equipment in turn. A large

[1] BCG x SIA, "Strengthening the global semiconductor supply chain in an uncertain era", April 2021.
[2] The die refer to the parts of the wafer on to which each chip is fabricated.

part of the cost of a fab is not the manufacturing equipment, expensive though it is, but the equipment for keeping everything inside the fab clean.

Why is cleanliness so important? The transistors on a modern chip are some few nanometres (nm) across. By contrast, a human hair is around 100,000 nm. Obviously, a hair ending up on a wafer would be a complete disaster, blocking thousands of transistors from being manufactured correctly and causing that die to fail. But it only takes something around 10 nm across to on the wafer to cause a die to (probably) fail. If a die is not manufactured correctly, it is simply thrown away. There is typically no repair process to fix it after it's made.

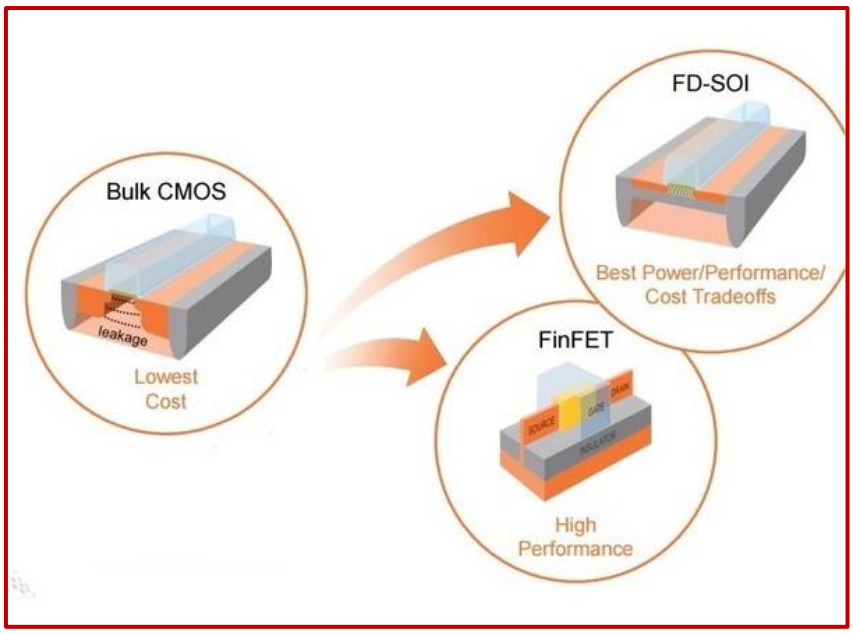
Annex 3. Moore’s Law



One famous representation of the processor industry is Moore's Law. This describes how the number of transistors in a chip doubles roughly every 18 months. This was true for a very long time, but is starting to slow down. Transistors are getting so small that we are nearing the limit of what physics will allow.

Annex 4. FinFET and FDSOI Semiconductor Technologies

Since the 1960s, the business of chip production has been driven by **doubling the number of transistors in a given area of semiconductor** and **hence doubling the computing power every eighteen months** (Moore's law). Complying with Moore's law requires **shrinking the feature size**[3] (28nm, 22nm, 16nm, 12nm, …)[4], increasing the wafer size (200 mm, 300 mm, …), or building vertically onto the chip (shifting from 2D to 3D architectures).



A major target in chip design and fabrication is to reduce and control the current - which activates the transistor gate[5] - and accordingly, the performance of the chip (switching speed & power consumption).

However, as transistors shrink, so does the proximity between its constituent components (the gate, source and drain). This gives rise to undesirable physical effects including loss of the gate's ability to control the current.

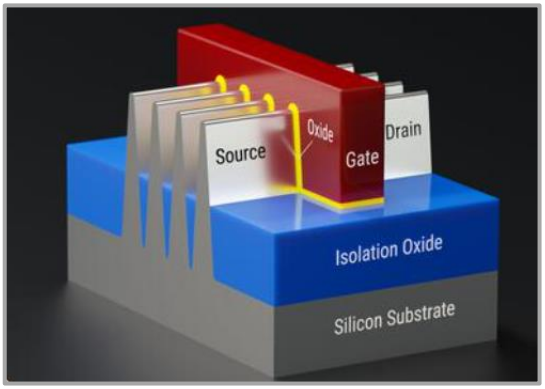
At process nodes below 28nm, transistors produced with conventional bulk CMOS technology no longer work because of these physical effects. This led to the development of alternative technologies, the most commonly used today being **FinFET** (fin field-effect transistor) and **FD-SOI** (fully depleted silicon on insulator), with **FinFET being the main technology of choice**.

These technologies differ in their **physical architecture,** which has a bearing on the respective fabrication processes. They also exhibit different **performance** characteristics, which will determine their suitability for a specific final application.

FinFET

A FinFET is a non-planar transistor where the gate is a fork-shaped 3D structure similar to a fish "fin" as shown in the figure. This architecture greatly improves the control of the gate over the current and thereby the switching of the transistor from on to off. FinFET requires a more complicated manufacturing process than conventional bulk CMOS with many more process steps needed to achieve the 3D structure.

[3] In semiconductor manufacturing, the process technology (or process node) determines the dimensions at which transistors can be printed onto a silicon wafer. Smaller process nodes produce smaller transistors; the smaller the transistors, the more you can fit on a chip and the faster and more efficient your processor can be.
[4] 1nm or 1 nanometre = 1 billionth of a metre.
[5] The gate switches the transistor on or off. A voltage applied to the gate controls the conductivity, and thereby the flow of current, between the source and the drain.

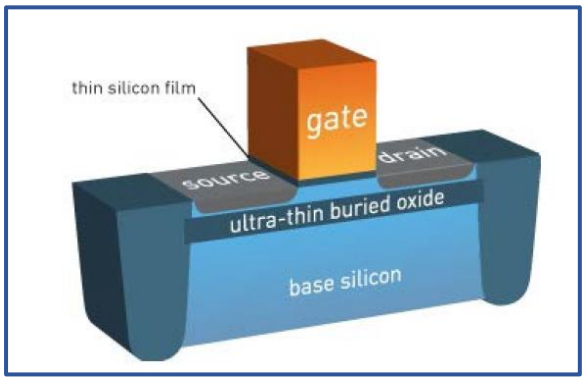


Chips utilizing FinFET have been on the market since the first half of the 2010s with Intel commercializing 22nm FinFET in 2011. With continuous optimization of the transistor density per chip, it has become the dominant design at 14nm, 10nm, 7nm and 5nm process nodes. The state of the art in FinFET is nominally 5 nm today, produced by TSMC and Samsung, with 3 nm in pre-production. Although European companies design in FinFET, they rely on foundries such as TSMC and Samsung for production.

FinFET devices are characterized by **fast switching speeds** and can support **high current densities** (present in heavily loaded circuits that operate 24/7).

FD-SOI

FD-SOI technology uses an ultra-thin layer of insulator positioned on top of the silicon substrate and a very thin silicon film as a means to better control the transistor behaviour. The architecture also enables the switching speed to be modulated dynamically during operation; this is a powerful means of optimizing power consumption when speed is less critical. Due to its planar structure, FD-SOI manufacturing is less complex requiring fewer process steps than FinFET.



Despite more costly[6] raw wafers (4 times more at around $400 rather than $100), the processed wafers are cheaper (some 7.3% lower for 14nm FD-SOI than for 16/14nm FinFET).

The simpler manufacturing process also makes it easier to add functionalities such as memory. The combination of memory and logic operations in a single process is attractive for applications at the edge of the network, including embedded AI in automotive and industrial manufacturing.

Currently, FD-SOI is in production at 28nm and 22nm (state of the art). Samsung has announced an 18nm node for which first production is expected in 2022. GlobalFoundries (GF) is developing 12nm FD-SOI at Dresden; it will be production ready in 2023-24.

FD-SOI exhibits excellent performance in terms of its behaviour at **radio frequencies (RF)** and its **reduced power consumption**.

Advantages and disadvantages

Both technologies have pros and cons and one may be inherently better than the other, **depending on the type of performance and requirements a specific application, product or system needs (speed, power consumption or cost)**.

[6] Due to the requirement that the silicon film and layer of insulator (buried oxide) need to be very thin and extremely uniform.

FD-SOI exhibits substantially reduced power consumption and is especially useful in lightly loaded circuits, like in IoT and portable/mobile applications, including automotive, where it enables longer battery life. Its RF variant, RFSOI, is used extensively in front-end modules (the interface between the transceiver and antenna) in smart phones and 4G/5G base stations.

FinFET will continue to be the technology of choice for applications with a lot of digital logic and that require the highest possible performance, like for HPC and supercomputing.

	FinFET	**FD-SOI**	
Base wafer cost		x4	SOI wafer cost ca. $400 compared to bulk Si $100, but finished wafer ca. $5000
Process complexity	↑	↓	FinFET ca. 40% more masks and process steps than FD-SOI
Overall/final wafer cost	→ to ↗	→ to ↘	finished wafer cost of 14nm FD SOI is 7.3% lower than that of 16/14nm FinFETs
Die yields	→ to ↘	→ to ↗	Yields higher with FD-SOI as bulk doping variability not an issue
Process control challenges	↑	↓	FinFET more complex
Transistor area density	↑	↓	Planar devices take more area
Performance/characteristics/cost	Higher performance, higher cost	Lower power, RF, lower cost	gate cost[7] for 14nm FD-SOI projected 16.6% lower than for 16/14nm FinFET

However, FD-SOI is well suited to achieving a **better performance / power consumption trade-off at functionally equivalent nodes.**[8] It is fair to say that the two technologies compete in many applications including automotive, AI, IoT, 5G/6G, and industrial manufacturing.

Developments

FD-SOI process technology has been developed and industrialized in Europe by CEA Leti, STMicroelectronics (ST) and Soitec in 28nm. These developments received significant support from the predecessor Joint Undertakings to KDT (ECSEL and ENIAC). Samsung and GF have licensed the

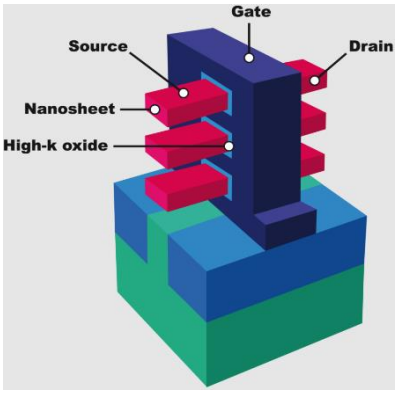
[7] The key cost factor for a customer is the "gate cost", a combination of the wafer cost, chip size and product yield.
[8] The 22nm FD-SOI technology exhibits similar performance to 14nm FinFET, with a lower production cost and researchers expect that 10nm FD-SOI will "likely" demonstrate similar performance to 7nm FinFET.

technology. There is a sizeable ecosystem in Europe that includes user companies such as NXP, Greenwaves, Valeo, Bosch and others as well as Racyics and Dolphin offering design services.

GF runs 22nm FD-SOI manufacturing lines in Dresden where it is also developing 12nm FD-SOI. The process has still to be optimized and will be production ready in 2023-24. Samsung has announced an 18nm FD-SOI node – for which first production is expected in 2022 - that might be a bridge to improved performance for customers using the 28nm node today. ST intends to license the 18nm technology from Samsung, integrate and further enhance it at Crolles. Such steps appear to be critical in enabling a route to 12/10nm nodes.

Scaling down FD-SOI technology to 10nm is expected to lead to significant improvements of chip performance compared to 22nm in terms of transistor density, power consumption, speed and RF behaviour. Transistor density can be improved by a factor of three and power consumption by a factor of two according to CEA-Leti. Research has shown that 10nm FDSOI will likely demonstrate similar performances in terms of transistor density, power consumption and speed to more advanced FinFET nodes such as 7nm, while maintaining its strong advantages for RF applications.

This would address the needs of a large part of the industrial market in Europe in the 2025-2027 time horizon, for example, for high-volume products like micro-controller units in the automotive and manufacturing industries as well as emerging markets in AI and communications.



While the path to 7nm FD-SOI is being *explored* in research settings - meaning there is *still much R&D work* to be done - 7nm and 5nm FinFET are already at volume production at TSMC and Samsung. 3nm FinFET is expected to reach mass production at TSMC in 2022 which is probably the limit for this architecture. Gate-All-Around Field-Effect Transistors (GAA-FET) - an evolutionary step from FinFET technology - will provide even better control of the gate over the current that is needed at these dimensions. TSMC is expected to release 2nm GAA-FET in 2023[9].

FinFET is without doubt a more mature technology than FDSOI, with scalability to lower node dimensions having been proven at industrial level. The equivalent scaling potential of FD-SOI has yet to be proven at volume production when it comes to node dimensions below 7nm.

[9] Samsung will use GAA-FET (nanosheet) also for 3nm - expected to be on track by 2022 for internal use (Samsung products) and made available to users through the company external foundry service in 2023.

Annex 5. Examples of ongoing Pilot Lines in EU

More-Moore Pilot Line

- Development of proprietary Extreme Ultra Violet (EUV) lithography equipment for sub 10nm nodes,
- Development of adapted Metrology technology for those nodes including failure analysis,
- Development of EUV mask technology,
- Development of process modules (lithography, etching, deposition, etc.) with eventual tool development) for sub 10nm nodes in mostly FinFET technology for the 3nm and 2nm research was also done on new device geometries.

FD-SOI Pilot Line

- Development and demonstration in an industrial environment of the Full Deplete technology on a SoI (Silicon on Insulator substrate) including
- Demonstration that FD/RF SOI is suited for ultra-low-power IoT[10] automotive, edge AI and 5G-6G devices.
- Demonstration that the higher wafer cost is offset by the simpler processing of the component, at a targeted low-power, ensuring the value and competitiveness of SOI technology for the related applications.
- The practical validation that back biasing enables clear gains for battery-powered applications, e.g. mobile computing.
- The complementary embedding of non-volatile memory
- The demonstration that RFSOI is a versatile solution that enables 5G front-end for frequency range beyond 6GHz, through the integration of switches as well as amplifiers on the same silicon substrates. This concept is in production in Europe on 200 mm wafer substrates[11].
- The demonstration of the SOI competitive advantage in higher frequencies (over 120GHz) on radar for automotive applications, which cannot be done with any other technology.
- The development of a rich ecosystem of design companies and end users, enabling the expansion of a strategic technology to maintain the European autonomy and leadership in relevant sectors, e.g. automotive, 5G/mobile communications, AI, IoT.

Pilot Lines for Heterogeneous Integration[12]

ECSEL supported many projects at different TRL levels in the domain of heterogenous integration, some pilot line projects are discussed below:

IoSense[13] consists of three interconnected semiconductor pilot lines in Europe: two 200mm frontend lines (Dresden and Regensburg) and one backend (Regensburg) line. This allowed to increase the manufacturing capacity of sensor/MEMS components by a factor of 10 while reducing manufacturing

[10] Internet of Things
[11] SRIA 2021, page 41
[12] According to the "Heterogeneous Integration Roadmap" by the IEEE Electronics Packaging Society (https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2021-edition.html), heterogeneous Integration refers to the integration of separately manufactured components into a higher-level assembly (System in Package – SiP) that, in the aggregate, provides enhanced functionality and improved operating characteristics.
[13] http://www.iosense.eu/

cost and time by 30%. The time for idea-to market for new sensor systems was brought down to less than one year.

MICROPRINCE[14] has created the first worldwide open access foundry pilot line for micro-transfer-printing (μTP) and demonstrated its capability for heterogeneous integration of different functional components in an industrial environment. Hence, cheaper and more miniaturized photonic integrated sensors systems could be fabricated based on the μTP process which will enable new medical diagnostic systems. This project is a nice example as to how pilot lines support the transfer of new technologies from the scientific and laboratory environment to an industrial environment bridging the "Valley of Death" to industrialization.

EuroPAT-MASIP[15] demonstrated the importance for Europe to develop an effective pilot line on Fan-Out Wafer Level Packaging (FOWLP) as an essential technology for heterogeneous integration of power electronics for a very diverse set of applications (from imagers to automotive electronics, through radars). Europe has little assembly and packaging capabilities as Asia leads in standard packaging. This pilot line demonstrated that it is possible to be competitive in advanced packaging and that is important to keep Europe competitive in microelectronics.

APPLAUSE[16] (Innovation Action though not a pilot line as such) develops specific high-value equipment for the heterogeneous integration of photonic components in an industrial environment, equipment that can be of use in a wide variety of other domains in heterogeneous integration.

InForMed, Position-II and Moore4Medical are a suit of pilot lines that realised the first pan-European infrastructure for manufacturing and assembly of small to medium volume of micro-fabricated medical devices in a complete innovation value chain from technology concept to high-volume production and system qualification. InForMed worked amongst other on advanced coating technologies for Bio-MEMS, POSITION-II on advanced Flex-to-Rigid technology, special sensors, etc. resulting in the smart catheter product. Moore4Medical implemented the **open-access offerings to the platforms**, which are being developed like multi-project runs in the semiconductor industry, expanding the technologies to microfluidics, organ-on-chip, silicon pump technology, etc. This environment is well suited to help start-ups launch innovative projects. Open technology platforms for specific domains are economically feasible, only if those platforms are conceived that they can also serve other application domains.

Photonics pilot lines

A new and promising field are photonic integrated chips. These devices integrate optical functions and optionally combine them with electronic function. The manufacturing volume is expected to grow significantly over the next years, making industrial exploitation viable (See for example Yole market report on Silicon Photonics[17]. European RTOs have developed state-of-the-art pilot lines for several technology platforms and are capable of low volume manufacturing. But industrial capacity is largely missing so far. The photonics21 partnership has under Horizon2020 supported following pilot lines which helped to get technologies closer to industrial level. These pilot lines are each distributed over several research centres and universities in Europe. In some cases companies which pioneer specific technologies also participate.

[14] https://microprince.eu/
[15] https://www.europat-masip.eu/
[16] https://applause-ecsel.eu/
[17] Silicon Photonics 2021 Market & Technology Report by Yole Développement (i-micronews.com)

Certain device types such as light sources are simpler to realise on Indium-Phosphide wafers (instead of Silicon). The project **InPULSE** strives to bring processing technologies closer to industrial maturity and establishes a platform to build chips which find applications in telecommunication and health[18].

The material Silicon Nitride allows the manipulation of visible light in wave guides with very low losses. This brings advantages for the miniaturisation of sensors for the health and food sector. The project **PIX4Life** has developed a platform for Silicon Photonics chips based on Silicon nitride[19].

Sensors and imaging systems working in the mid-infrared range of light are ideal to detect gases with high very high precision and sensitivity. The Pilot line project **MIRPHAB** has developed technologies to package the relevant optical and electronic components in an package ('system in package') and offers a platform to bring these into industrial application[20].

The packaging of integrated circuits with optical functions is very complex and in need of modularization and standardization to bring down costs and increase reliability. The pilot line project **PIXAPP** has been working on a system platform that makes it simpler for industrial users to pick and tailor processes to their needs[21].

Other projects have established research pilot lines to improve the manufacturing of micro-lenses[22], medical components using light technologies[23] and organic LEDs on flexible substrates[24]. The challenge for all pilot projects is to make the step to high-volume manufacturing which requires buy-in and investment of industrial partners. R&I measures are envisaged under this Act which should help to bridge the gap to industrial uptake.

Graphene pilot line

The 2D-EPL project has established a pilot line for prototype production of graphene and related materials (GRM) based electronics, photonics and sensors, based around prototyping services (in the form of Multi Project Wafer runs as well as tailor designed integrations) for 150- and 200-mm wafers, based on the current state-of-the-art graphene device manufacturing and integration techniques. This will ensure external users and customers are served by the 2D-EPL early in the project and guarantees the inclusion of their input in the development of the final processes by providing the specifications on required device layouts, materials and device performances. The consortium will develop a fully automated process flow on 200- and 300-mm wafers, including the growth and transfer of high crystal quality graphene and TMDCs. The project will cover the whole value chain including tool manufacturers, chemical and material providers and pilot lines, to secure progress in GRM integration and to be able to offer prototyping services to academics, SMEs and companies which can benefit from the progresses of GRM integration with silicon achieved within the 2D-EPL consortium.

[18] InPulse - JePPIX Pilot Line - SMART Photonics

[19] Silicon Nitride Photonic Integrated Circuit Pilot line for Life Science Applications in the Visible Range | PIX4LIFE Project

[20] Home - Mirphab

[21] Packaging Solutions - Pixapp

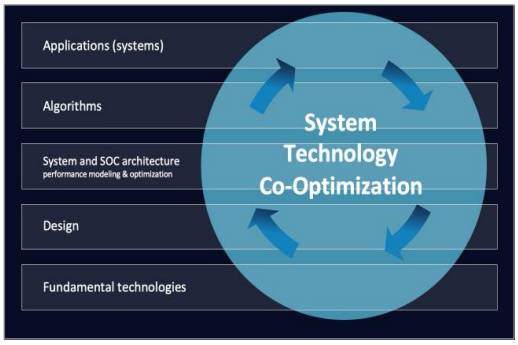
[22] PHABULOuS Pilot Line for free-form micro-optics

[23] Home | Medphab

[24] Lyteus

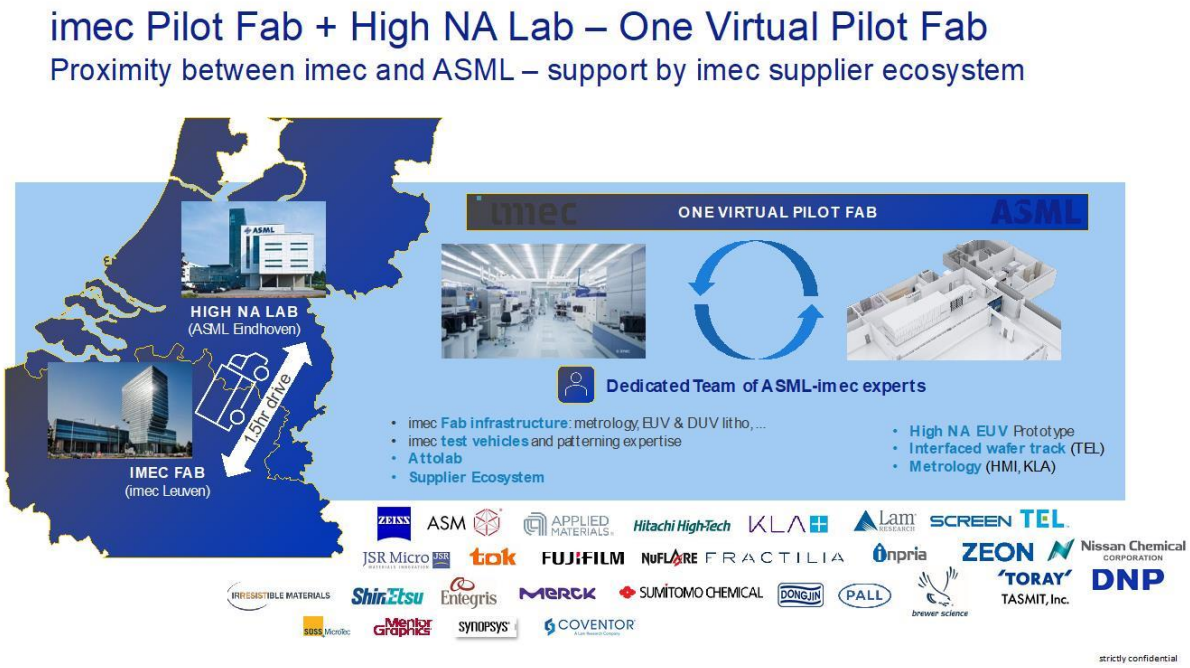
Annex 6. Chips for Europe: Examples of impact of Pilot Lines

More than ever, equipment & material suppliers are playing a key role in collectively tackling the scaling challenges posed by today's fast-evolving, capital equipment-intensive, complex semiconductor landscape. Strong R&D interactions between manufacturers and suppliers at an early stage of development accelerate technology advancements and optimize the return on investment for all partners involved. The close partnership with leading systems and application companies fuels the methodology of design & system co-optimization, that is key to the multi-domain and multi-scale innovation power brought by **advanced pilot lines facilities**.



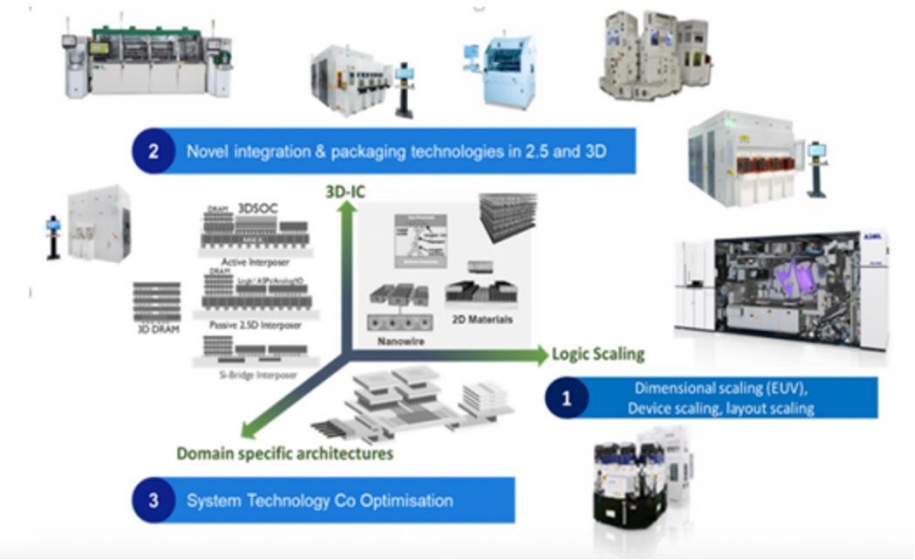
Example #1: The Suppliers' hub

The Chips for Europe's key asset for the European Materials and Equipment suppliers is the suppliers' hub infrastructure. One example is the High-NA EUV research from imec in partnership with ASML. This research is unique in the world and its results will be essential for implementing advanced node logic and memory innovation. Another example is the development of Atomic Layer Deposition, which has become the world standard for deposition of high-k dielectrics and metal gates, and which has been pioneered through early European collaboration of ASM and imec.



Bringing together advanced equipment and materials manufacturers in **a pre-competitive processing facility** offers the opportunity to perform the pathfinding for the process module options of the next-generation technology nodes mentioned above as well as for equipment and materials manufacturers to gain early feedback on their product roadmaps. The imec suppliers' hub, including the ASML partnership, is exemplary for the success of this operational model. A similar hub to support FD-SOI technology at CEA-Leti is also a clear example.

The European suppliers' hub will be a facility that is unique in the world for demonstration and integration of new process modules and that strengthens the European leadership in critical process steps, such as leading-edge lithography, 3D integration, materials, wafer technologies and metrology, sustainability, automation etc. The availability of an extended facility, which allows the individual process modules to become part of a full flow, at appropriate integration density, is of extreme importance to validate the process options and intellectual property valuation.



Leading equipment and materials suppliers can only optimize their tool performance by performing high-value module validation using an industry-relevant pilot line setting, requiring access to the most advanced leading-edge process modules. They achieve this validation by participating in individual innovation programs embedded in an industry-relevant R&D facility, providing the necessary feedback during the equipment development cycle.

Example #2: Exploring the impact of Backside Power Distribution Network on high performance chips

The goal of a power delivery network of a chip is to provide power as well as a reference voltage to the active devices on the die. This network is essentially a network of interconnects that is separate from the signal network. Traditionally, both networks are fabricated through back-end-of-line (BEOL) processing on the frontside of the wafer. But we can also choose to move the power distribution to the backside of the silicon wafer, which today serves only as a carrier. This would allow direct power delivery to the standard cells, and promises to enhance system performance, increase chip area utilization, and reduce BEOL complexity.

ARM, in collaboration with imec, earlier showed the beneficial impact of using backside power delivery as a scaling booster in the design of a central processing unit (CPU). Using backside power delivery turned out to be the most efficient way of delivering power to the circuits. ARM and imec implemented a Cortex A53 CPU design using a future 3-nanometer process developed by imec. It largely improves on the supply-voltage drop that is caused by the resistance in the BEOL of traditional designs. In the 'winning' processor design, the backside power delivery is connected to a buried power rail, a structural

scaling booster in the form of a local power rail that is buried in the chip's front-end-of-line. (https://spectrum.ieee.org/arm-shows-backside-power-delivery-as-path-to-further-moores-law)

However, the realization of true backside power delivery networks comes with additional technological complexities, that are tackled at the pilot line facility. A dedicated wafer thinning process is needed in combination with the ability to process nano-through-silicon-vias that electrically connect the backside to the frontside of the device wafer. The work in imec's pilot line showed progress in developing the critical technology building blocks needed for realizing backside power delivery networks as a structural scaling booster to further the path of Moore's Law. Furthermore, it has been shown that the wafer's backside can create a very dynamic design space with new design options to optimize the power delivery for scaled systems. A perfect example of where a system-technology co-optimization (STCO) will bring very exciting new perspectives for high-performance systems.

This is an interesting example of how new modules can make a difference in system performance, but it requires however to set up the virtual prototype facility to allow for meaningful experiments. In the last section of this document, we explain the flow and characteristics of a professional virtual prototyping infrastructure that will be provided by the Chips for Europe initiative.

Example #3: embedded non-volatile memories for IoT and edge AI

Intrinsic Semiconductor Technologies Ltd ("Intrinsic") has successfully scaled its silicon oxide-based resistive random access memory devices (RRAM) and **demonstrated electrical performance characteristics that will enable their use as high-performance, low-cost, embedded, non-volatile memory in logic devices at advanced processing nodes on imec's pilot line**.

Together with imec, Intrinsic's RRAM devices have been successfully scaled to dimensions of 50 nanometres and have demonstrated excellent switching behavior, which is key to their use as the next generation of non-volatile, solid-state memory. This milestone confirms that the devices are compatible with the advanced semiconductor manufacturing process nodes used across the semiconductor industry, both in terms of physical dimensions (scaling) and electrical performance characteristics, making them suitable for use in Edge AI and IoT applications.

According to Nigel Toon, advisor to Intrinsic and CEO, Graphcore: "Intrinsic is on track to offer a new, embedded, non-volatile memory that is compatible with the most advanced semiconductor process nodes, an option that doesn't exist today.

https://www.semiconductor-digest.com/intrinsic-announces-breakthrough-as-memory-devices-successfully-demonstrated-at-commercially-relevant-nanometre-scale/

Example #4: Europe can become a leader in microdisplays for the ER/VR era

On March 22, 2022 MICLEDI Microdisplays announced an agreement with GlobalFoundries to Collaborate on MicroLED Displays for AR Glasses. MICLEDI Microdisplays, a 2020 spin-off from imec, develops microLED displays for next generation Augmented Reality (AR) glasses. MICLEDI's vision is to enable AR for everyday personal use - smart glasses that are small, lightweight, with long battery life, and at reasonable cost. To make this happen, MICLEDI is developing the world smallest and brightest displays. The key innovation behind MICLEDI is the **new integration technology for microLED on 300mm wafers developed in the pilot line facility with imec.**

MICLEDI Microdisplays, a leading developer of microLED arrays for augmented reality glasses, today announced a manufacturing collaboration with GlobalFoundries (GF) to enable AR glasses to achieve

the brightness, resolution, power, size, and economies of scale needed to be attractive to mainstream consumers. Under the agreement, MICLEDI's solution will be combined with GF's 22FDX® feature-rich platform that provides the leadership performance, ultra-low power and broad feature integration capability needed to build MICLEDI's microLED arrays in mass production. Such companion integrated circuits (ICs), which can be customized for different customer applications, will provide the image processing, driver and control functions needed to complete the display modules using wafer-to-wafer hybrid bonding.

"We are pleased to collaborate with GF as we move from pilot-line manufacturing to mass production in a world-class fab," said Sean Lord, CEO at MICLEDI Microdisplays. "To enable optimum microdisplays for AR, MICLEDI has developed a unique and innovative solution for microLED manufacturing integrating both the controller IC and emitter module to leverage GFs 300mm semiconductor manufacturing technology, capitalizing on manufacturing precision for product performance, high volume and low-cost."

https://www.micledi.com/news/press-release-jan-9th-2020

https://www.micledi.com/news/press-release-march-22nd-2022

Example #5: A technology highly specialized technology module can make all the difference: Hyperspectral imaging

With the advent of more compact hyperspectral cameras and real-time hyperspectral imaging, a set of new applications comes to light. Some examples:

- **agriculture** – Often mounted on drones, light-weight hyperspectral cameras can detect the smallest differences in plants or soils and inform farmers and researchers about diseases, droughts, and so on.
- **machine vision** – Automated industrial processes such as classification, error detection and sorting benefit from a technology that can clearly and quickly distinguish superficially identical entities.
- **medicine** – Thanks to real-time hyperspectral imaging, it's now possible to use hyper-spectral imaging to inspect living tissue, for instance in diagnostic tools or during surgery.
- **art and heritage** – Historical artefacts have many stories to tell. The challenge is to uncover their secrets without touching, and sometimes even moving them. That's where portable, high-resolution hyperspectral cameras come in.
- **remote sensing** – More and more observational satellites leave for space with a hyperspectral sensor on board. It enables them to make out the spectral signatures of soil, vegetation and mineral.
- **forensics** – Hyperspectral imaging's ability to detect spectral fingerprints includes those of materials such as blood or gun powder. It identifies such markers at a crime scene without using chemicals that could tamper with the evidence.

The imec hyperspectral technology has been licensed to the imec spin-off Spectricity, which is a fabless company creating spectral sensing solutions for high-volume and mobile devices, using CMOS technologies. After the phase of pilot line low volume manufacturing, the company is now looking at doing its test production in a European speciality foundry.

Example: Machine vision

In just three years, French company Tridimeo produced a highly precise 3D vision solution for industrial robots. The solution is three times faster than the current industry standard and gives precise "sight" to robots, thereby improving quality checks, picking, and placing parts in challenging lighting conditions. Tridimeo combines 3D and multispectral capabilities to equip manufacturing robots with a robust and reliable set of eyes. The company uses imec multispectral sensors for their solution. **Imec assists in ramping up the production of the sensor now that the start-up company shifts to deployment on an industrial scale.** Renault is Tridimeo's first customer.

Example #6: Specialty components for specific high value – low volume markets

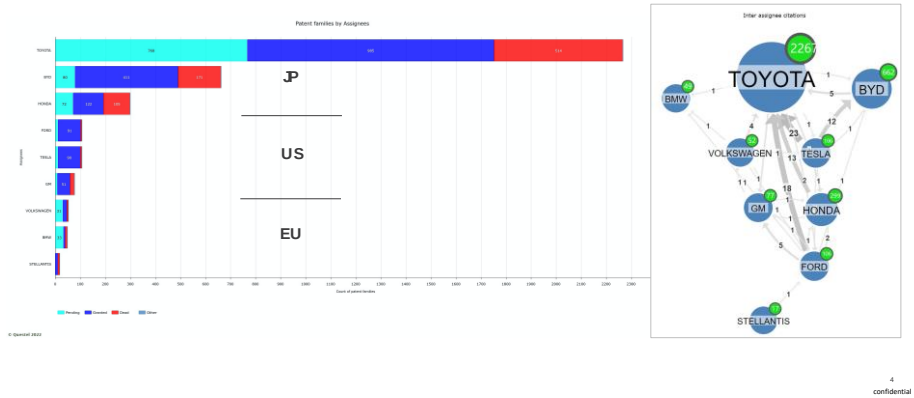
In 2011, Imec announced that it successfully qualified a chipset consisting of custom high-quality EUV sensor dies. These are now being integrated in ASML's NXE:3100 EUV lithography tools in the field, improving the tools' overlay and critical dimension tool performance. The sensors were processed according to ASML's custom designs and specifications, with focus on superior lifetime and sensitivity to direct and high EUV irradiation doses. Two of the sensors are designed to calibrate, align, and focus tool's lens systems. A third sensor is designed to monitor the NXE:3300's EUV dose.

This example confirms that an advanced pilot line can be capable to provide partners with custom specialty chip solutions. Indeed, **a pilot line can offer companies all the services needed to turn innovative ideas into smart packaged microsystem solutions with a wide variety of device technologies** (e.g. CMOS, Si-photonics, MEMS, image sensors, packaging ...). The applications include strategic areas such as bio-sensing, energy- and power management, and high-end specialty imaging, photolithography among others. The pilot line services can range from feasibility studies over design and technology development to prototyping and low-volume manufacturing. And through a strong alliance with the existing foundry and IDM landscape, technology transfer will enable volume production in line with the market demand.

Example #7: IP 'opportunity' in the Automotive

A first analysis of intellectual property creation classified under "semiconductor" in Automotive companies over the period 2010-2020 shows very interesting statistics. The left figure shows the number of semiconductor patent filings by the three largest automotive companies in terms of market cap in Asia, the U.S. and Europe. The right graph shows to which extent the selected patents serve as prior art for each other.

Toyota has filed many patents on semiconductors and further analysis will need to detail the underlying patent family streams but an early start on electrification is most certainly an underlying aspect. Toyota is clearly a technology leader as their patents are prior art for many automotive companies. While the sheer size of Toyota's patent portfolio certainly drives this result, it is apparent that for 1 out of 5 patents by Tesla or Ford a Toyota patent is prior art, while this is barely the case for EU automotive companies, indicating that the technology portfolios of U.S. automotive companies are closer to Toyota than the technology portfolios of EU automotive companies.



Notes: The graphs show patents with a priority date between 2010 and 2020 that are classified under the International Patent Classification H01L (~semiconductor devices).

The U.S. automotive companies come behind Asia but before Europe in semiconductor patent activity. This ranking holds both in the absolute number of patent filings, as well as in relative numbers when we look at the ratio of semiconductor patent filings to total patent filings by automotive companies. When looking at filing trends over time, it is noticeable that there is an uptake in Ford's semiconductor patents from 2015 onwards, while at European companies the uptake in semiconductor patents is less outspoken. European car manufacturers clearly have another strategy since they are relatively absent on the patenting scene in this category and probably largely rely on their Tier-1 and Tier-2 suppliers for semiconductor innovations. While this has worked in the past when semiconductors were less central in the innovation of automotive – though were essential in differentiating functions such as safety features, microcontrollers and various sensing and imaging functions and of course entertainment – the future is different. The car will be an HPC cluster on wheels with the semiconductor innovation at the heart.

The pilot line facility can help to innovate through the full stack of the ecosystem and provide winning intellectual property to the automotive industry in leading-edge technologies through virtual prototyping and early system impact innovation.

Example #8: Next Generation Communications Infrastructure

As stated by Alexandros Kaloxylos, Executive Director of 6G-IA, "The role of micro-electronics in the evolution of telecommunication networks and services is undeniable. As Europe should keep its leading position in telecommunications, the impact of microelectronics in the ICT sector is of prime concern for the members of the 6G-IA. Thus, it is vital to identify future telecommunication networks' technologies and their requirements from the underlying hardware infrastructure."

An ongoing roadmapping exercise (CoreNect) with partners from across the telecommunications industry such as Nokia, Ericsson, NXP and ST clearly states that with its strong position in the infrastructure market and research, its expertise in material science, and the existing fabrication capacity, Europe could become an IC design and fabrication powerhouse. However, it is repeatedly mentioned that the packaging level will require advanced PCB technology or heterogeneous 2.5D / 3D integration. As several European companies and research groups (among which the large RTOs imec,

CEALeti and Fraunhofer) are strong in this domain, a transfer of this know-how to the industry is an opportunity for Europe to play a stronger and critical role at a higher level in the supply chain than solely at the level of chip design and processing. This is an area where virtual prototyping and early access to pilot lines are key to prove out the co-design of technologies.

A first example from the wireless space is in the mobile network's energy of which 80% is consumed by base station sites. In particular, the composing chipsets. or systems-on-chips (SoC), are major contributors to the energy consumption. The base station systems for beyond 5G hence need to be highly energy efficient on the one hand, but on the other hand they also need to handle extremely high data rates, should not introduce high processing latency and provide sufficient flexibility for features like dynamic spectrum sharing. (https://www.bell-labs.com/collaboration-opportunities/d-a-p/collaborations-ku-leuven-and-imec-push-state-art-energy/). Together with imec, Nokia Bell Labs have developed a novel way to partition the SoC's on-chip memory system and to drastically reduce the energy consumption. In order to achieve an optimal partitioned architecture, we have devised a simulation platform that allows a fast design-space exploration.

A second example is the collaboration with CST Global on disruptive, integrated silicon photonics systems which benefitted from early access to a pilot line-like technology. Anders Storm, CEO of Sivers IMA, said, "The integration of imec's advanced SiPho technology platform with our indium phosphide (InP) DFB lasers and InP reflective semiconductor optical amplifier (RSOA) Photonics solutions, has already demonstrated excellent results. We expect that these new light sources will encourage the uptake of SiPho devices in a wider range of cost-sensitive, industrial markets. The collaboration between the exceptional design and manufacturing team at our Photonics unit, CST Global, in Glasgow, UK and imec's world-leading research and innovation hub in nanoelectronics and digital technologies, will allow the creation of disruptive, integrated SiPho systems with superior performance and reduced cost." (04/03/2020)

In general, it is expected that next-generation wireless and wireline communication systems will bank on a combination of both very high speed, highly scaled digital nodes and novel material systems. A design infrastructure which combines virtual prototyping with a pilot line to verify the critical differentiation steps for European technology integration would multiply opportunities as shown above.

Example #9: supporting innovations through realization of companies ASIC ideas. (EUROPRACTICE example)

Wiyo is a Spanish Internet of things (IoT) start-up that created an intelligent tag to enable simple and efficient solutions in the world of automatic identification and data capture. When you put the Wiyo solution in any object or physical element, you can immediately interact with, sense, and follow that object in real time – regardless of whether it's moving or stable. Consider it an RTLS (real-time location system) and IoE (Internet of Everything) solution without a battery and with no dedicated readers. Any generic Wi-Fi source can power and enable the interaction. The solution has countless possibilities and lots of industries can take advantage of it (smart hospitals, smart stores, smart food deliveries, Industry 4.0, ...). When it became clear that this solution needed a chip, Wiyo contacted the imec.IC-link team that gave support/advise throughout the whole flow of the ASIC development from technology choice up to building the capacity to test the chip, improving the design for future manufacturing, and adding design for testing to get ready for mass production.

(https://www.imeciclink.com/en/articles/start-doesnt-have-time-or-money-make-mistakes)

Turning company ASIC ideas into real products can be a complex process. By utilizing its partner network, imec.IC-link offers a complete range – from ASIC design to product qualification (use of EDA tools, technology and design support, standard packaging for test chips and extensive training). Once the company is ready to fabricate its ASIC design, Imec.IC-link assists with flexible access to multi-project wafer (MPW) and volume production at leading foundries for mature and advanced nodes, including its own innovative technologies such as gallium nitride and silicon photonics.

It is expected that the technology in the next decade will be even more complex than it is today and as such the way of working that is in place at imec.IC-link is seen as a good starting point for attracting and supporting customers of the pilot lines.

Example #10: supporting the industry in the area of Fan-Out Wafer Level Packaging

Heterogeneous integration is one of the most promising ways to bridge the gap between emerging microelectronics and its derived applications, both are pushing new packaging technologies. New technology architectures are needed to integrate the progress made in nano-electronics, wireless technologies and photonic component technologies into electronic systems. Fan-out wafer level packaging (FO-WLP) or panel level packaging (FO-PLP) is now the optimal result of the merge between single-chip and multi-chip packages. The evolution of single chip packages (SCPs) has started from small metal boxes and developed for dual inline packaging (DIP) for through-hole assembly and surface mount technology (SMT) packages such as the quad flat package (QFP) to the ball grid array (BGA). BGA packages use rigid or flexible interposer for the redistribution from the peripheral pads to the area array. The minimum packages size has been achieved with WLP because the package size is equal to the die size. For all these packages OSATs are needed for SMEs. Due to the nature of standardized packages even small companies and R&D institutes are supported in this are by small volume offers. Further advanced packages are based on embedding technology. The main advantages of FO-WLP and FO-PLP are the substrate-less package, lower thermal resistance, higher performance due to shorter interconnects together with direct IC connection by thin film metallization instead of wire bonds or flip chip bumps and lower parasitic effects. Especially the inductance of FO-WLP is much lower compared to FC-BGA packages. In addition, the redistribution layer can also provide embedded passives (R, L, C) as well as antenna structures using a multi-layer structure. Therefore, FO-WLP are used for multi-chip packages and can be viewed as a synergy between optimal chip package and the MCM concepts. Hence, technology is well suited for heterogeneous integration which is only possible on wafer or panel scale. Unfortunately, small volumes are not offered by OSATs due to wafer or panel scale fabrication. Therefore, a multi-project approach is extremely needed to open the advantages of these packages also for SMEs.

Fraunhofer has started an international consortium to explore the potential of this technology. After the international Panel Level Consortium 1.0 has achieved the overall goals of the project in 2019 with significant technical progress in the field of large area Fan-out Panel Level Packaging a new consortium has been formed to continue the development with a focus on ultra fine-line routing including R&D on migration effects. The project has started 1st of February 2020 and will run for two years. Partner which have signed for the consortium up to now are: Ajinomoto Group, Amkor Technology, ASM Pacific Technology Ltd., AT&S Austria Technologie & Systemtechnik AG, BASF, Corning Research & Development Corporation, Dupont, Evatec AG, FUJIFILM Electronic Materials U.S.A., Hitachi Chemical Company, Ltd., Intel Corporation, Meltex Inc., Nagase, RENA Technologies GmbH, Schmoll Maschinen and Semsysco GmbH.

Example #11: High density interconnect for highest bandwidth at lowest power

Future electronic systems like autonomous systems using high performance computing (HPC) and edge computing systems, sensor integrated systems and bio-integrated devices will require more and more functions which cannot be managed by a single chip, even if advanced SoC (System on Chip) concepts are used. Heterogeneous integration will be the next step and will pass beyond current SiP (System in Package) approaches.

A main bottleneck is the efficiency of data handling between computational processing units and memories. As an example today's supercomputers run at about 5% or even less of their theoretical computing power due to the limited memory bandwidth New hardware and software architectures are necessary to break down the boundary between pure logic and pure memory domains. One very suitable approach hereby is the split up of the different logic building blocks into chiplets. In that way, the connections can be optimized in respect to increase bandwidth bottlenecks. Furthermore, the yield of very complex processing units results in extreme increasing costs alongside with further front end node miniaturization in the IC manufacturing process. This can be overcome by the use of chiplets which means that IP blocks made in different technology nodes will be combined on an interposer to reduce cost by increasing the production yield (smaller chips) and reuse across applications. Different technology options are possible for routing the high density lines on the substrate: Si-Interposers are already proven as a possible but high-cost solution, high density organic substrates with or without embedding technologies and the different variations of Fan-Out packaging approaches using molded substrates with embedded active components. With the emerge of sub-7nm technologies, also the need to merge CMOS cores with non-CMOS technology will become necessary for cost and performance reasons in medium term, increasingly. Therefore, the concept of chiplets which split such difficult-to-make functional blocks into modules that are more manageable, will mainly benefit from this new interconnection technologies.

In short-term heterogeneous integration will appear at chip, package and organic substrate or panel level. The main physical advantages are the lower thermal resistance, higher performance making it ideally suited for RF applications like 5G and beyond. Extreme high density interconnect approaches such as hybrid bonding in combination with TSVs push the limits regarding CMP-capability in back end and placement accuracy with the potential to replace microbump flip-chip assembly in long-term for highest performance applications. Therefore, the development and standardization of active Si-interposer concepts using hybrid bonding for chiplets using sub 1 µm interconnection precision is necessary for electrical and physical interface standards for data rates into the TB/s regime with energy efficiencies down to 0,2pJ/bit and ns latency for high performance computing. Future electronic systems will be based on increased functionality requiring not only the integration of different technologies but also optimization with respect to reduced carbon footprint and low energy consumption. Highest reliability and long lifetime for autonomous systems will be key for economic success keeping an optimized balance between cost and performance. Hardware /software co-designs must be the result as an Assembly Design Kit (ADK) for new complex packages like wafer and panel level embedding for further miniaturization, enhanced functionality, and increased energy efficiency. Looking on the technological variety and their demands for high performance applications, there will be a significant impact on the package supply chain in the industry. Whereas strict separation of front end, OSAT and substrate suppliers dominated the past, these boundaries seem to vanish more and more as the need for miniaturization to keep up with Moore's law cannot be fulfilled by node miniaturization alone and will be distributed alongside the supply chain. This is especially valid for packages in the field of high performance applications like IoT and edge devices in the era of AI.

Example #12: Exploring the Green Potential of New Advanced Packages

Packaging of electronic components is often considered a small addition to the manufacturing of the core functionality of the component. In particular, for semiconductors, or integrated circuits (ICs), the majority of investments, developments and personnel will be focused on manufacturing the highest performing chips with the smallest reproducible features in huge cleanroom facilities. Packaging, on the other hand, is not core business and has typically been outsourced or shifted away to former low wage countries in Asia, such as the Philippines or Malaysia . Conventionally, the cost of packaging is only a few percent of the component costs, and likewise – though few studies reveal data publicly – packaging will only contribute a few percent to the environmental profile of a component. Current research in the field of environmental assessment and cost modeling of microelectronic manufacturing indicates that with advanced packaging technologies and the prominent example of chiplets, the value contribution of packaging increases and in some cases can suddenly contribute dominant effects. These effects would appear both in economic analysis and environmental impacts. The implications are two-fold: chiplets could deliver substantial improvements (i.e. lower impacts for same or higher functionality), but could also introduce new critical materials and increase environmental impacts per delivered functionality.

In summary, a new IC packaging paradigm introduces new processing steps and new materials in the production stage in order to drive miniaturization and performance forward, while keeping the costs balanced to the performance gains. Therefore, on the one hand, environmental analysis on an in-depth technical level is needed to determine the environmental effects of introducing a new packaging technology, such as chiplets. On the other hand, we need to make sure that environmental practitioners identify and assess multi-chip packages correctly to begin with.

Example #13: Packaging DfR (Design-for-Reliability) Toolbox

The Vision:

Mission profile adapted functional product qualification

Standardised common mission profiles

Structured database of characterised available technologies and models

Why does the industry need a DfR Toolbox now?

Shortening product cycles and shortening of development times

Extended lifetime requirements (i.e. automobile electrification)

Diversity of application and packaging scenarios (IOT, 5G, Robotics, …)

Use of COTS in Non-Consumer application (need for requalification)

Increasing sensitivity of consumers (i.e. Premature Obsolescence)

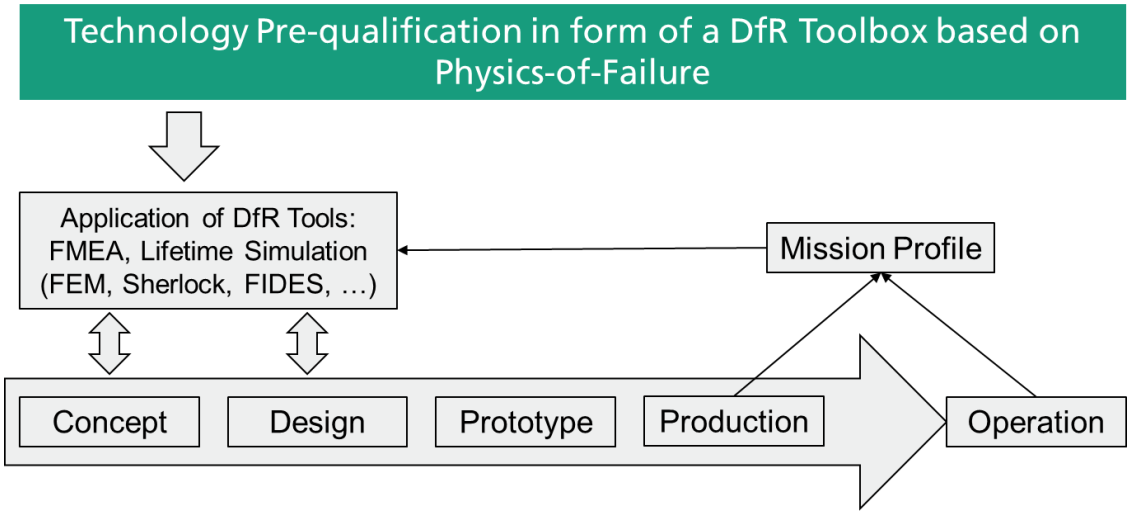
Outcome

Early access to know-how on leading-edge technology robustness

Special technology lifetime models

Acceleration factors / activation energies and validation of lifetime models

Models for early design evaluation usable in design tools (e.g. Sherlock)



How Virtual Prototyping on the pilot lines works

The goal of designing a virtual prototype is to explore system-level impact of the proposed innovative semiconductor integration technology and manufacturing options at component and IP-block level, at system-on-a-chip level or even at board or blade level.

In this context, the design is implemented using infrastructure that consists of the PDKs (process design kits) and EDA (electronic design automation) flows that represent the proposed innovative semiconductor integration technology and manufacturing options.

The virtual prototype then allows a validation of the value proposition and trade-offs in terms of materials, device, design, and architecture options.

This requires that the PDKs are mature enough to support the complete design flow from RTL to GDS. The design infrastructure must be complete enough to evaluate PPAC at a level that shows non-trivial impact and complex ROI calculation of basic innovation questions. The digital part of a PDK has many hundreds of cells, of which almost all are needed to implement a CPU as well as memory primitives and structure compilers. The design infrastructure includes geometry rules needed to implement significant analogue circuit IP, such as SERDES, PLLs and specialized I/O cells, as well as tools for analogue design, RTL synthesis, logical equivalency, ERC/DRC, etc.

A pilot line is the enabling manufacturing infrastructure necessary for realizing hardware to calibrate and correlate with the model assumptions.

There is a very close interaction between the activities executed on the pilot lines and the practice of virtual prototyping. A virtual prototype addresses critical technology-related questions like “Is the device performance meeting expectations?"

Note, this **does not** imply that the entire virtual prototype is “taped-out” in the “pilot line”, but rather identifies critical constituents at the level of a logic gate, or critical process module, or part of integration stack that **informs critical PDK** implementation parameters. These parameters are then used to

finetune the PDK parameters of the virtual prototype creating a feedback loop between virtual prototype and manufactured samples.

Design infrastructure is also a critical piece of the equation. Without design-infrastructure enablement there is no fundamental connection between the complex trade-offs at the level of significant IP architecture and micro-architecture and the technology development and improvements that are achieved in the pilot fab through technology innovation.

These design infrastructure critical skills are required to realize the custom PDKs and implementation extras that are used to implement virtual prototypes and guide the complex DOE (Design of Experiments) trade-offs that are needed in the pilot line. **One cannot minimize the fundamental need for this capability and its tailored nature to a particular technology implementation. More crisply: the skills needed to implement PDKs and virtual prototypes are fundamentally tied to the technology DOEs and have to be part of the same organization.**