Monitoring semiconductor value chains: Implications for International Cooperation

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1. Purpose of the report

The semiconductor world is rapidly changing, and this brings along challenges for Europe and other regions in the world.

The mission of the European project ICOS (International Cooperation On Semiconductors), is to identify the needs and opportunities for international collaboration in this changing ecosystem. Its main objective is to support the European Commission in its efforts to re-establish Europe's global position in the semiconductor value chain, as advocated by the European CHIPS Act, by identifying topics where research cooperation with leading semiconductor countries could be beneficial for the growth of the European industry. The project explores how the EU can collaborate with different countries around the world to tackle a list of common challenges.

Published in July 2024, the report "*Economic analysis of the EU and International semiconductor ecosystem*" (D2.1), led by DECISION Etudes & Conseil for the ICOS (International Cooperation On Semiconductors) project:

a) Offers a comprehensive overview of the semiconductor ecosystems in leading global regions (EU27, USA, China, Japan, South Korea, Taiwan, India, Malaysia, and Singapore).

b) Establishes a foundational analysis for exploring potential areas of cooperation between the EU27 and each of these regions (confidential).

The objective of this follow-up report, *"Monitoring the Semiconductor Value Chain: Implications for International Cooperation",* is to provide an overview of the key evolutions of the international environment between 2023 and 2025 that might impact Europe's cooperation with third countries in semiconductor:

1. Geopolitical Landscape and Strategic Implications for the Semiconductor Value Chain. How has the geopolitical landscape evolved since 2023? What implications does it have on trades and for potential cooperation with third countries?
2. Status of Semiconductor Investment Plans. How have investment plans evolved from January 2024 to June 2025? What implications could this have for potential cooperation with third countries?
3. Status of Semiconductor Talent Gaps. What are the current semiconductor talent gaps within the EU and other regions? What opportunities for cooperation could address these gaps based on complementary strengths?

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This report also presents **the results of the Survey on international cooperation opportunities for the semiconductor industry in Europe** launched in March 2025 by ICOS partners CEZAMAT WUT, UGent and Fraunhofer.

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2. The Semiconductor Value Chain in a Shifting Geopolitical Landscape

Since 2023, geopolitical developments have significantly impacted the organization of the semiconductor value chain. Tariffs, export controls or bans, and investment restrictions now shape supply chain strategies, leading many companies to adopt "local-for-local" manufacturing models.

2.1.A Globalized Semiconductor Value Chain: The State of Play in 2025

By the early 2020s, after three decades of globalization largely free from geopolitical constraints, the semiconductor industry had become the most globalized of all value chains—defined by an unprecedented level of regional specialization.

While most design capabilities remained concentrated in the United States—or were outsourced to India—the rise of fabless and fab-light models shifted manufacturing to Asia, which by 2025 hosted 81% of installed front-end[1] capacity and over 85% of back-end capacity[2].

[1] In the semiconductor industry, the front-end refers to the manufacturing of integrated circuits on silicon wafers, typically carried out in cleanroom fabs using photolithography, etching, and deposition processes. The back end refers to the subsequent stages of cutting, packaging, testing, and assembling the chips, usually performed in separate facilities and involving different industrial players.

[2] Data from SEMI, Q4 2024.

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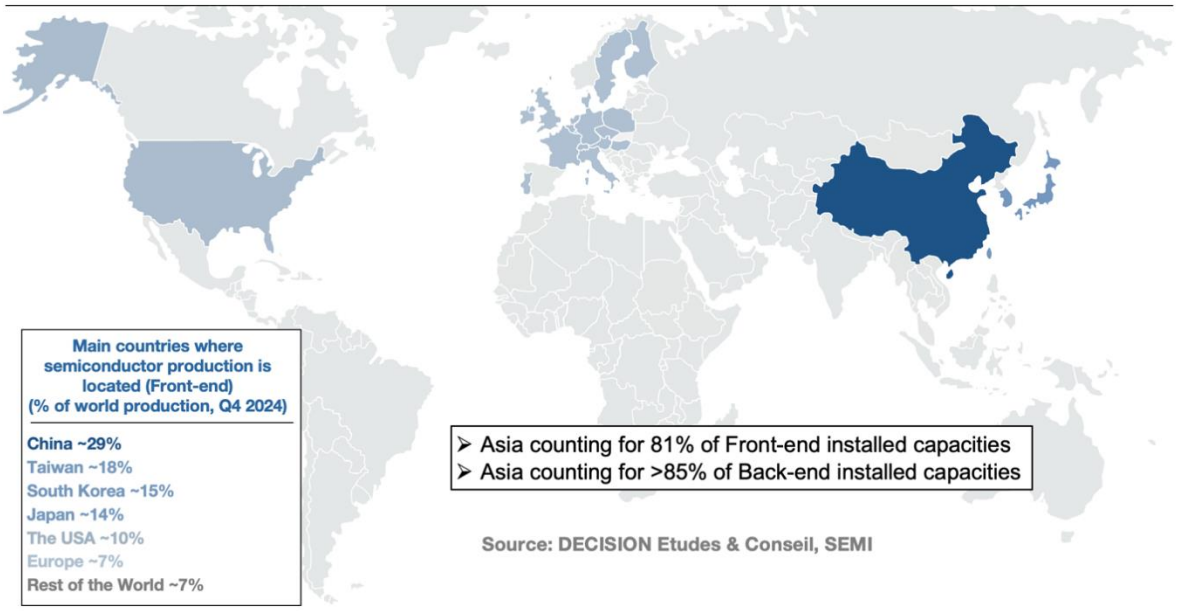
Figure 1: Semiconductor Manufacturing Installed Capacities, Q4 2024



Source: DECISION Etudes & Conseil, SEMI

As shown on Figure 2, the United States—historical leader and birthplace of the semiconductor industry—remains the only country with end-to-end capabilities across the entire semiconductor value chain. Its few weaknesses have been addressed through the CHIPS Act, notably via: (1) large-scale investments in advanced processor fabs by TSMC, Samsung, and Intel, and (2) a € 9 billion raw wafer facility by GlobalWafers in Texas[3].

[3] Printed Circuit Board (PCB) manufacturing remains a key dependency, with only 3% of PCBs produced on U.S. soil, while more than 60% are manufactured in China, according to Data4PCB.

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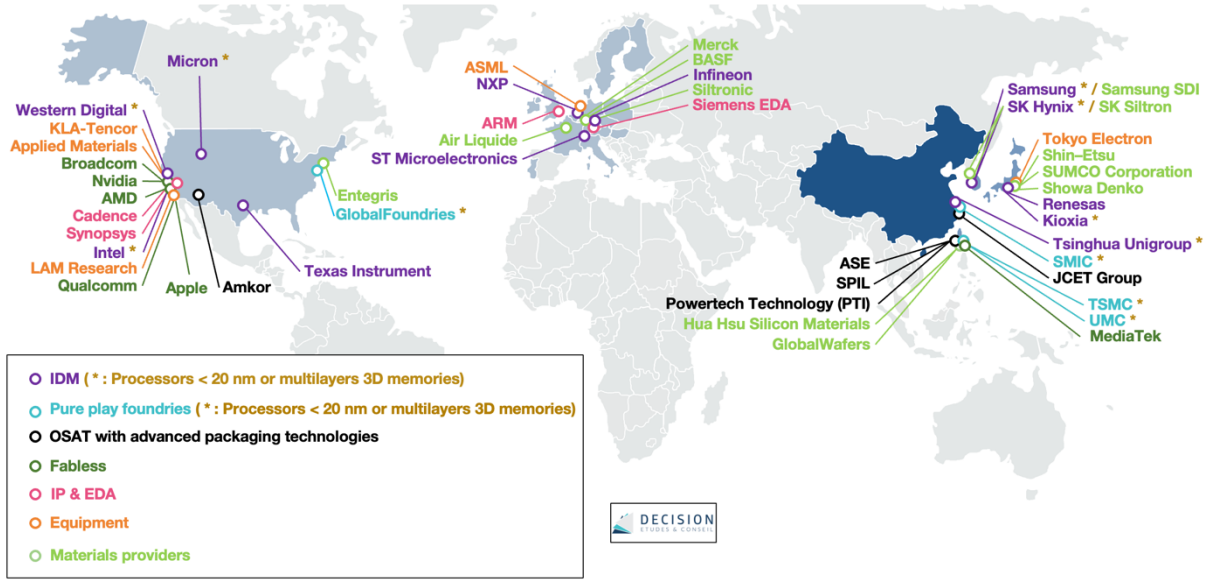
Figure 2: Global Semiconductor Landscape in 2024



Source: DECISION Etudes & Conseil

Since launching the "Made in China 2025" initiative in 2016, China has been the only country—aside from the United States—to pursue end-to-end control of the semiconductor value chain. In response, the U.S. has since 2018 deployed an expanding arsenal of trade and investment restrictions, alongside diplomatic pressure, to slow China's progress.

Figure 3 below compares the positioning of the United States and China along the value chain. Green bars indicate market share held by domestic companies; red bars show production share located on national territory.

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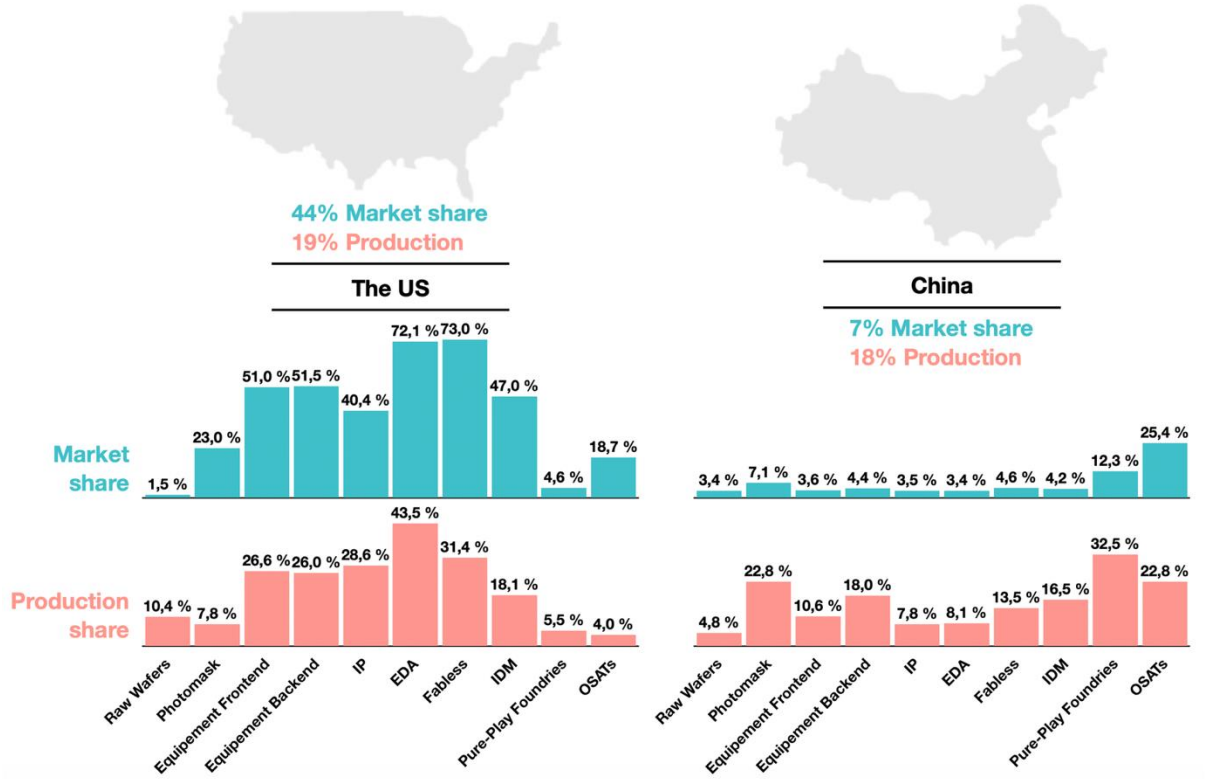
Figure 3: The US and China: The Only Two Countries Aiming to Control the Entire Semiconductor Value Chain



Source: DECISION Etudes & Conseil, data for year 2022

This figure highlights the weakening of the U.S. position in the manufacturing segments of the value chain—such as raw wafers, photomasks, foundries, and OSAT—after decades of pursuing fab-light and fabless strategies. In contrast, China is leveraging the strength of its manufacturing base across all segments—largely established by non-Chinese companies—to build a robust domestic ecosystem. National and local governments actively support dozens of firms in every segment, often in competition with each other.

In terms of semiconductor ecosystem located on national territory, China has already caught up with the United States. In 2022, 19% of global manufacturing along the semiconductor value chain (measured by installed capacity or employment) was located in the U.S., compared to 18% in China—placing both countries as the world's two leading semiconductor ecosystems, on equal footing.

However, in terms of global market share held by domestic firms, China still lags significantly behind. In 2022, U.S. firms captured 44% of global market value across the

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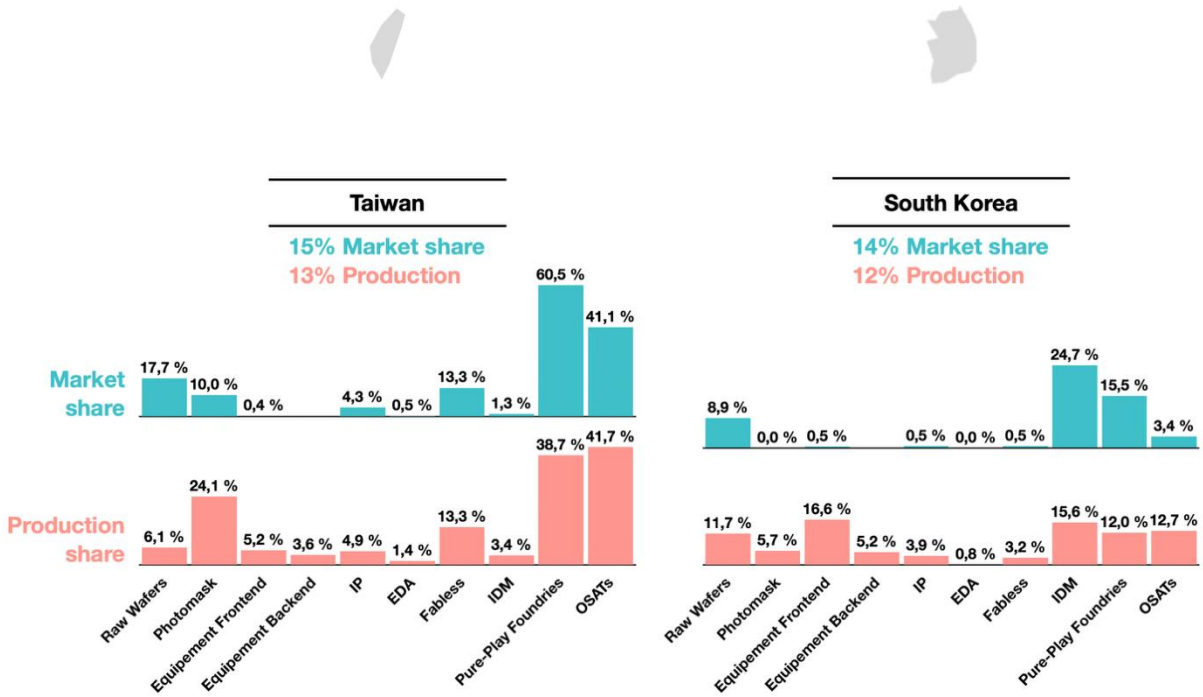
value chain, while Chinese firms accounted for just 7%. Yet China is catching up fast and is projected to become the second-largest country by market share before 2035.

As detailed in Figure 4, Taiwan and South Korea are the two leading countries in the manufacturing of processors, logic, and memory chips—across both front-end and back-end stages. Taiwan also has a significant strength in photomask production, while both countries play a notable role in raw wafer manufacturing.

South Korea benefits from Samsung's strong design capabilities, and Taiwan's design ecosystem is growing, fueled by firms like MediaTek.

Figure 4: Taiwan and South Korea: The Two Leading Countries Leading in Semiconductor Manufacturing



Source: DECISION Etudes & Conseil

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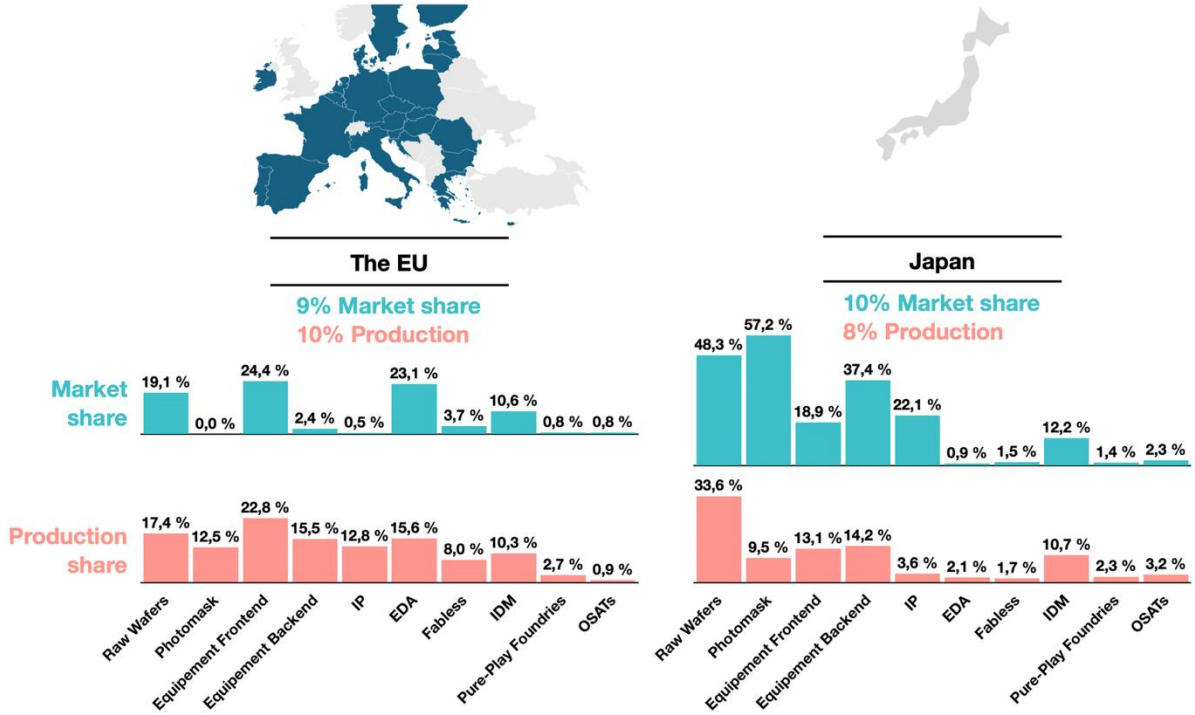
As shown in Figure 5, The European Union and Japan are in relatively similar positions, with historically strong ecosystems—particularly in IDMs serving embedded markets, as well as in semiconductor equipment, materials, and tool suppliers—and a clear determination to preserve both market share and manufacturing capabilities.

Figure 5: The EU27 and Japan: Historical strengths in IDMs, Equipment, Materials & Tools



Source: DECISION Etudes & Conseil

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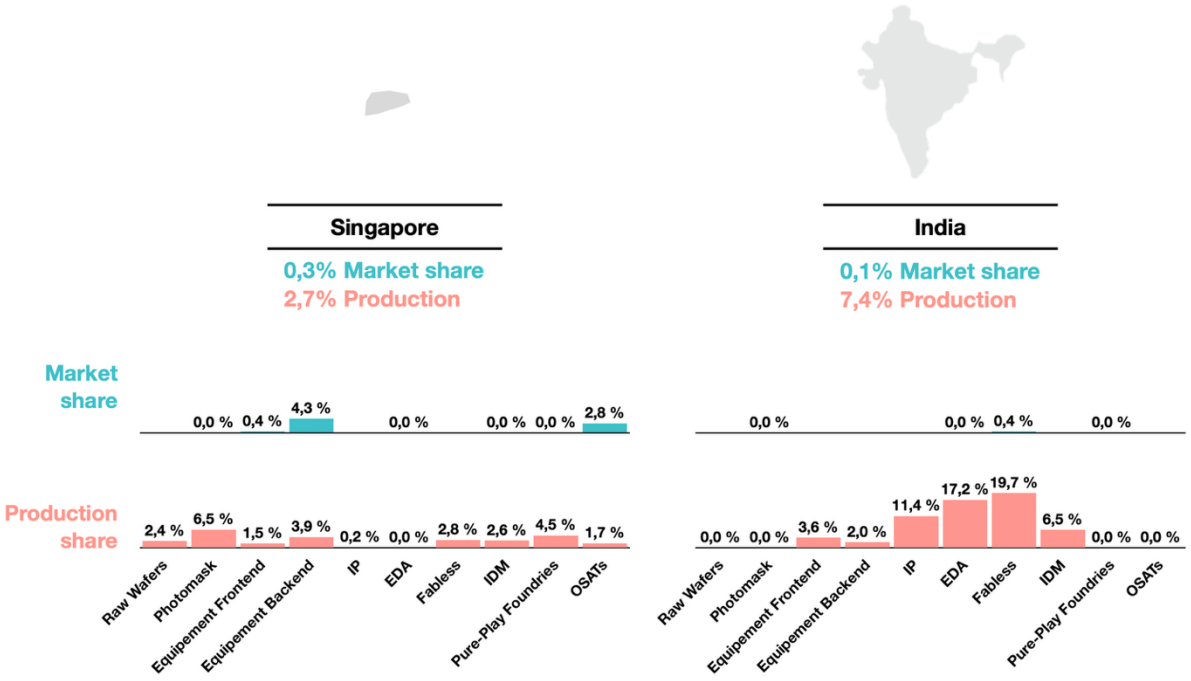
As detailed in Figure 6, Singapore has emerged over the past few decades as a semiconductor hub, featuring a domestic ecosystem that includes OSAT providers, back-end equipment manufacturers, semiconductor production facilities—particularly from European firms—a skilled workforce, and targeted R&D activities.

Finally, India is the latest emerging player in the semiconductor industry. After decades of attracting fabless companies, it has become the second-largest country—after the United States—in terms of employment in fabless, IP, and EDA firms.

In 2019, India introduced its first National Policy on Electronics, aiming to develop a domestic ecosystem across the entire value chain. Following years of difficulties in attracting foreign investment—largely due to infrastructure challenges—India secured its first major back-end investment in 2023 with Micron, and its first front-end investment in 2024 with the PSMC-Tata partnership. The year 2024 also marked the launch of the first SEMICON India, attended by Prime Minister Narendra Modi, as well as the first EU–India R&D cooperation workshop under the ICOS framework.

Figure 6: Singapore and India: Rising Semiconductor Ecosystems



Source: DECISION Etudes & Conseil

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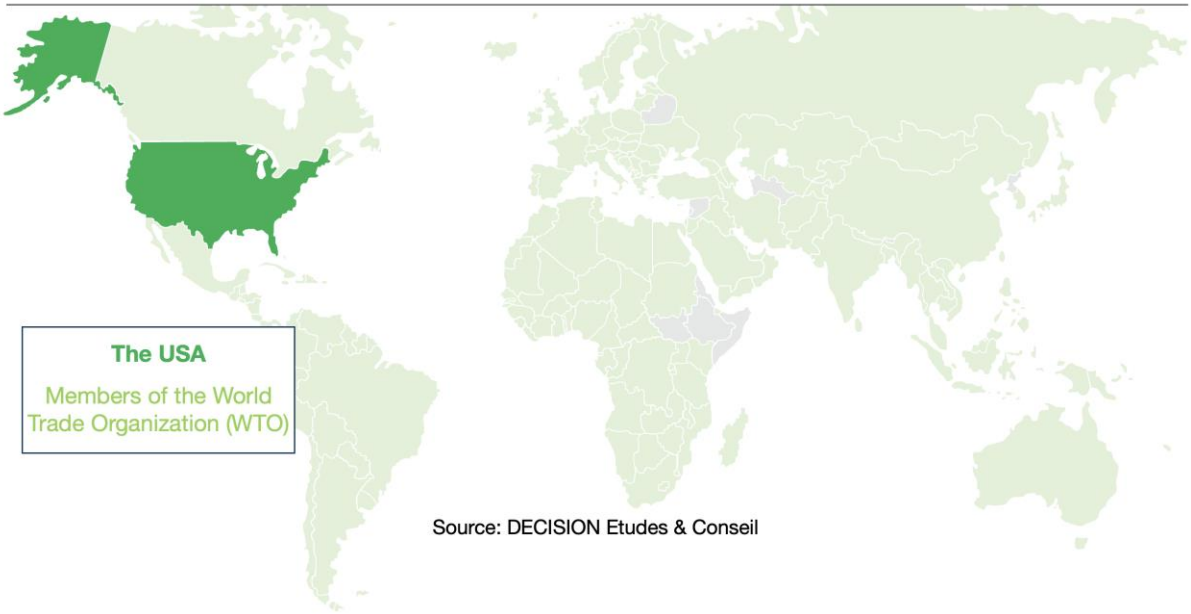
2.2.1990s-2020s: A shifting Geopolitical Environment

2.2.1. The End of Globalization in a Unipolar World

This single, globalized semiconductor value chain—characterized by deep country-level specialization—is the result of 27 years of development by companies serving a unified global market without geopolitical constraints on their supply chains.

This was enabled by U.S. dominance in a unipolar global order, supported by successive free trade agreements under the World Trade Organization (WTO), which counted 164 member states by 2018.

Figure 7: 1991-2018: 27 years of globalization in a unipolar World



Source: DECISION Etudes & Conseil

Starting in 2016, China's ambition to gain full control over its semiconductor value chain—coupled with growing U.S. efforts to prevent this—marked the beginning of a new geopolitical era.

2.2.2. The Road to Multipolarity

However, a broader power shift from the West to the Global South had already begun in the early 2000s. The figure below illustrates this transition. It shows the evolution of industrial value added between 2000 and 2023 for three blocs: the G7, the BRICS, and the Strategic Triangle. The figure below illustrates this transition. It shows the evolution of industrial value added between 2000 and 2023 for three blocs: the G7, the BRICS,

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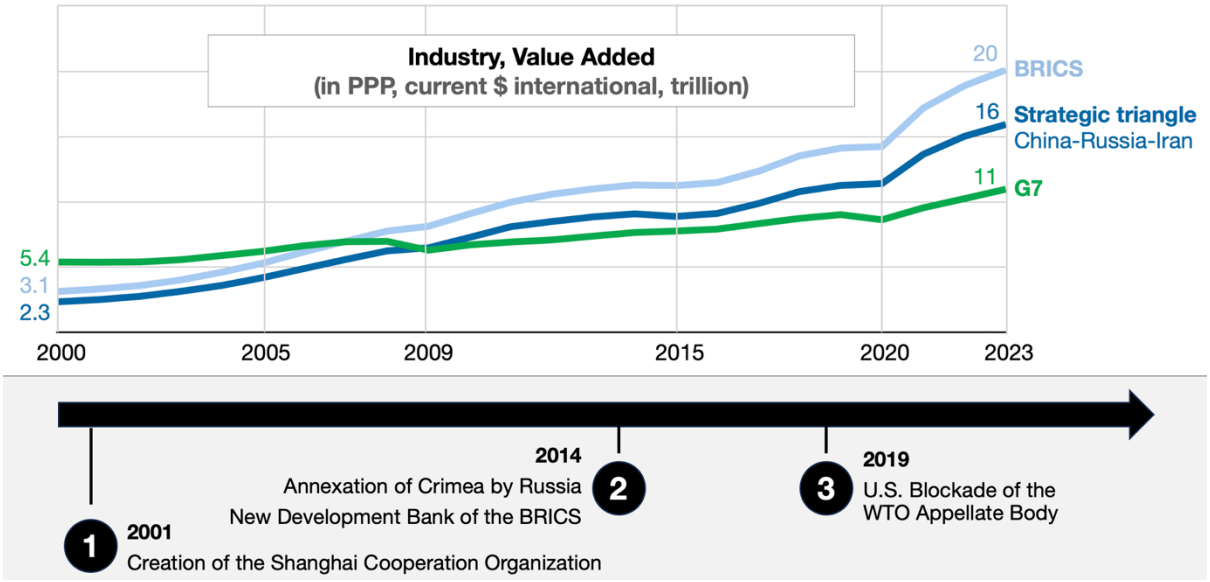
and the Strategic Triangle[4]. In 2000, the G7's industry was twice the size of the Strategic Triangle's and 1.5 times that of the BRICS. By 2023, the situation had reversed: the BRICS bloc had twice the industrial value added of the G7, and the Strategic Triangle outpaced the G7 by 50%. Underlying this broader industrial shift is the semiconductor market, which has also moved increasingly toward Asia.

Figure 8: 2000-2023: Towards multipolarity



Source: DECISION Etudes & Conseil

In parallel with this industrial shift, the 2000s and 2010s were also marked by a series of initiatives that signaled a move toward multipolarity—either through the creation of new international organizations or through strategic decisions taken independently of U.S. influence.

A first milestone came in 2001 with the creation of the Shanghai Cooperation Organization (SCO), a permanent intergovernmental body aimed at strengthening mutual trust and good neighbourly relations among its Eurasian member states, and promoting cooperation in political, economic, cultural, and security affairs. While the SCO's official mandate does not explicitly advocate a multipolar world order, it has progressively functioned as a platform for coordination outside Western-dominated frameworks—thus indirectly contributing to a more multipolar global landscape.

Another major initiative followed in 2013 with the launch of China's Belt and Road Initiative (BRI), which began establishing new transport and logistics infrastructure across

[4] This term designs the alliance between China, Russia and Iran.

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Eurasia and beyond, with the potential to reshape global trade routes and reduce dependence on traditional maritime corridors.

In 2014, the creation of the BRICS New Development Bank provided a concrete alternative to the World Bank, while Russia's annexation of Crimea marked a major geopolitical rupture.

In parallel, many BRICS+ and SCO countries began to pursue dedollarization strategies and have since developed alternatives to the U.S.-controlled SWIFT system for international payments.

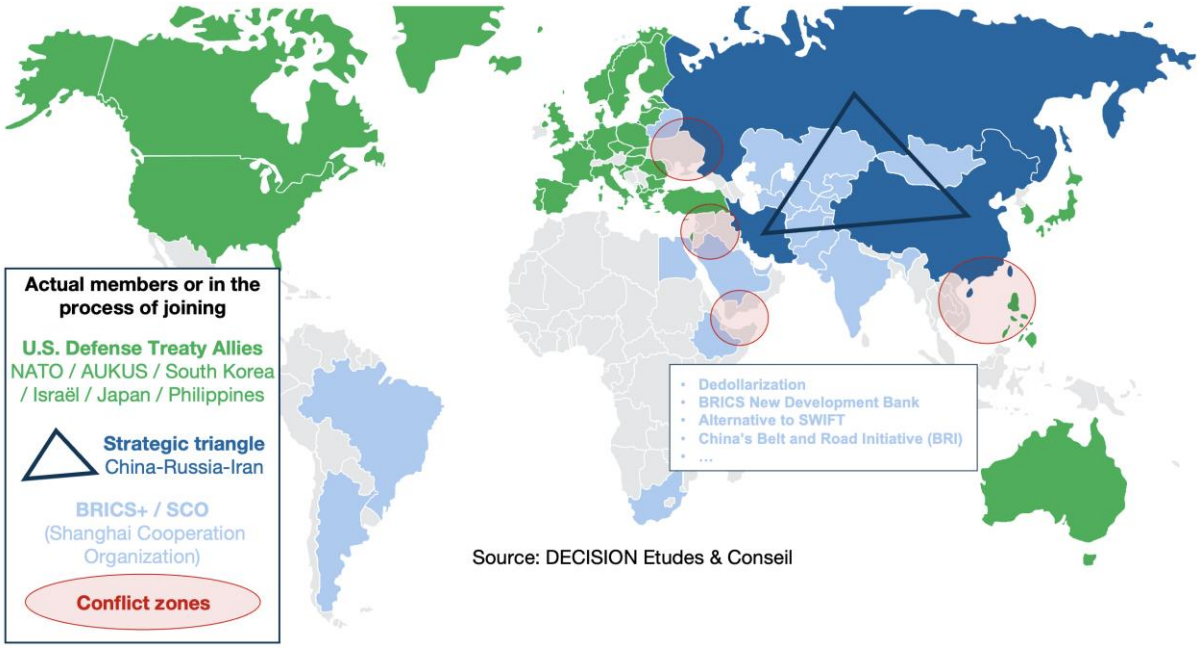
Finally, in 2019, the United States' blockade of the WTO Appellate Body effectively paralyzed the global trade dispute settlement mechanism, signaling the end of the post-Cold War momentum toward rules-based free trade.

As a result, while the United States retains significant influence, it faces increasing constraints in imposing its strategic preferences on third countries. This applies to the semiconductor value chain—especially in light of the rise of Chinese and Taiwanese semiconductor ecosystems.

2.2.3. 2018-2024: Towards a logic of blocks?

Between 2018 and 2024, global geopolitics gradually shifted toward a bloc-based order—most aptly captured by the narrative of "the West versus the Rest".

Figure 9: 2018-2024: Towards a logic of blocks? The West versus the Rest?



Source: DECISION Etudes & Conseil

The Biden administration worked to consolidate U.S. treaty allies into a cohesive strategic front—spanning NATO in Europe, AUKUS in the Pacific, and broader Indo-Pacific coordination with Japan, South Korea, India, Australia, and the Philippines—to counterbalance China's growing influence.

The U.S. withdrawal from the Iran nuclear agreement in 2018, followed by the war in Ukraine starting in 2022, accelerated the rapprochement between Iran, Russia, and China. Simultaneously, Russia and China were officially designated as systemic rivals in U.S. national security strategies and policy discourse.

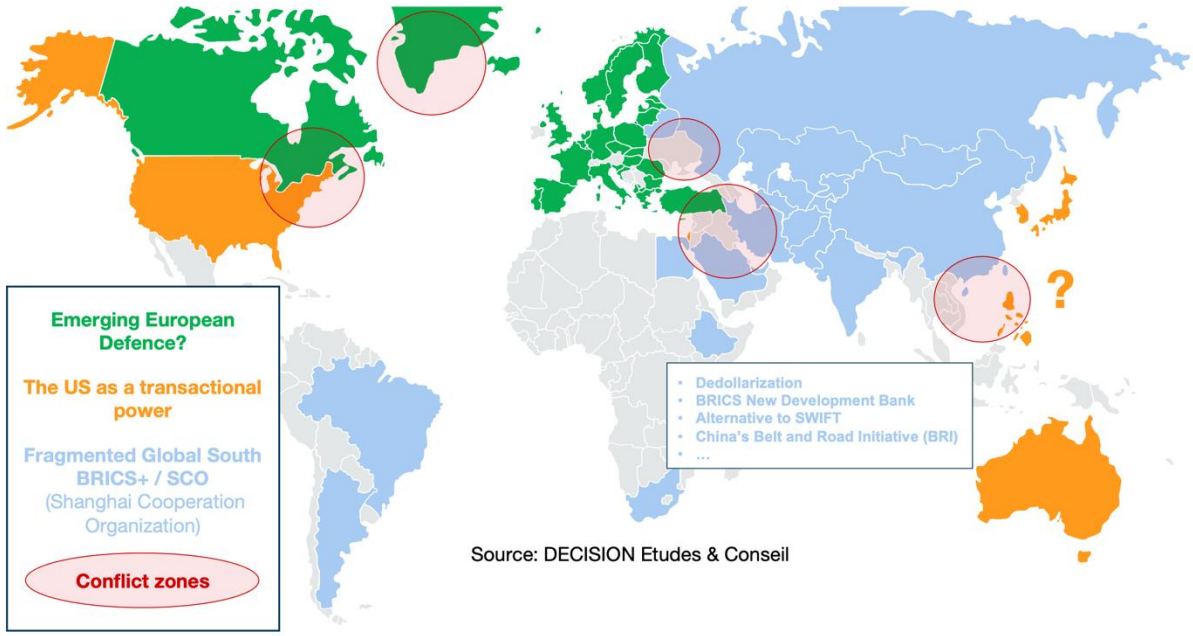
In Europe, NATO gained renewed momentum from 2022 onward, marked by increased defense spending, enhanced political cohesion, and the accession of Finland and Sweden.

2.2.4. Since 2025: A World of Fragmentation & Multipolarity

Donald Trump's return to the U.S. presidency in 2025 marked a turning point in global geopolitics.

Rather than reinforcing a unified Western front, the second Trump administration embraced a transactional foreign policy—favoring bilateral deals aimed at maximizing U.S. advantage, often at the expense of traditional alliances.

Figure 10: Since 2025 – A World of fragmentation & multipolarity



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Source: DECISION Etudes & Conseil

In Europe, this shift reinforced the sense of a "post-Munich world," where increasing calls for a more autonomous European defense policy questioned the continent's reliance on NATO.

In the field of semiconductor cooperation, this shift has led the European Union to recalibrate its strategic partnerships—placing greater emphasis on deepening ties with Taiwan, while discussions on transatlantic coordination have seen less momentum.

2.2.5. Regionalization of Value Chains and the Logic Behind U.S. Decoupling Strategy

Despite political changes, the U.S. has pursued a consistent strategy since 2016—based on a clear diagnosis and a dual-track response to reduce dependence on China.

The assessment. The free-market policies of the 1990s led to a single, deeply integrated global semiconductor value chain. This system now underpins the entire U.S. industrial, digital, AI and defense ecosystem. However, in the event of reunification between China and Taiwan, China would control 67% of global back-end capacity, 47% of front-end capacity, and 66% of capacity above 5 nm—rendering the U.S. dangerously dependent on Chinese-controlled production with no short-term alternative.

The strategy. The U.S. has pursued two complementary goals:

1. Reduce China's role in the global semiconductor supply chain through export controls, export bans, investment restrictions, and diplomatic pressure.
2. Rebuild a secure, China-free value chain by reshoring production through domestic initiatives such as the CHIPS Act and the IRA, and by collaborating with trusted international partners via frameworks like ITSI or the OECD.

These efforts have contributed to the **progressive decoupling of the global semiconductor supply chain into at least two branches: one serving China, the other the United States**. As a result, companies have, over the past 5 to 10 years, increasingly adopted **"local-for-local" manufacturing strategies**, at minimum for the U.S. and Chinese markets, and in some cases systematically across all markets.

This momentum is likely to continue over the coming decades and will shape the geopolitical trajectory of Taiwan. As the United States works to reduce its dependence on the *Taiwanese silicon shield*, China is investing massively in its military capabilities in order to shift the balance of power and achieve reunification with Taiwan without provoking U.S. military intervention. The Chinese strategy appears aimed at achieving

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reunification without military confrontation, possibly in several decades once the balance of power shifts decisively. In the meantime, TSMC's continued expansion in Taiwan pushes that horizon further into the future, which helps explain U.S. efforts to pressure the company to prioritize production on American soil, where 65% of its customer base is currently located.

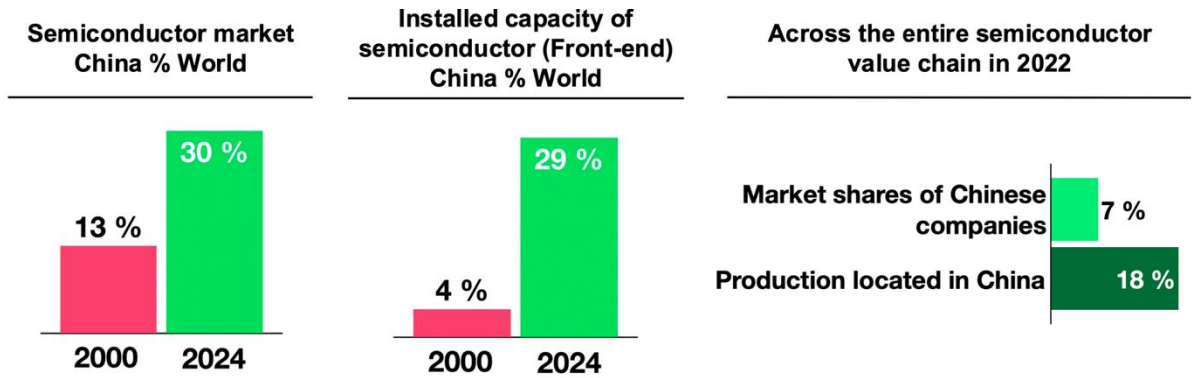
2.3.Semiconductor: China's Rise and U.S. Industrial Policy Tools Aimed at Containment

2.3.1. The rise of China

China's 2015 "Made in China 2025" strategy marked its first formal commitment to mastering the entire semiconductor value chain. A decade later, the results are striking. Between 2000 and 2024, China's share of global semiconductor consumption rose from 13% to 30%. Over the same period, its share of installed front-end manufacturing capacity surged from 4% to 29%.

More significantly, China has now effectively matched the United States as the world's leading semiconductor ecosystem, with a 2022 production share across the value chain of 18%, compared to 19% for the U.S. China's next objective is to expand the market share of its domestic semiconductor firms—an effort already showing rapid results across all segments.

Figure 11: Semiconductor: The rise of China



Source: DECISION Etudes & Conseil, WSTS, SEMI

2.3.2. U.S. Efforts to Contain China's Rise

Since 2016, the United States has implemented a progressively assertive strategy to limit China's ascent in the semiconductor industry. This strategy, which blends trade restrictions, legal mechanisms, and industrial policy, aims to curb China's access to

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advanced technologies while reshoring and consolidating control over critical parts of the global semiconductor value chain.

Building the Legal Architecture of Technological Containment

The policy shift began with an expansive interpretation of existing U.S. legislation, notably the Foreign Corrupt Practices Act (FCPA), which was increasingly used to investigate foreign companies deemed strategically sensitive and, in some cases, to facilitate their acquisition by U.S. investors.

In parallel, tighter control over cross-border capital flows was made possible by the 2018 Foreign Investment Risk Review Modernization Act (FIRRMA), which broadened the mandate of the Committee on Foreign Investment in the United States (CFIUS). These changes allowed U.S. authorities to block a series of high-profile Chinese attempts to acquire semiconductor-related firms, including Aixtron, Lattice Semiconductor, Siltronic, and Lumileds.

Beginning in 2016, the United States initiated trade restrictions targeting China's access to critical technologies. The primary instrument was the Entity List, maintained by the Bureau of Industry and Security (BIS), which allows the U.S. government to impose export bans on designated companies and products. In 2016, only three Chinese entities linked to the electronics sector were included. By June 2022, that number had grown to 201 Chinese organizations, and it has continued to increase each year since.

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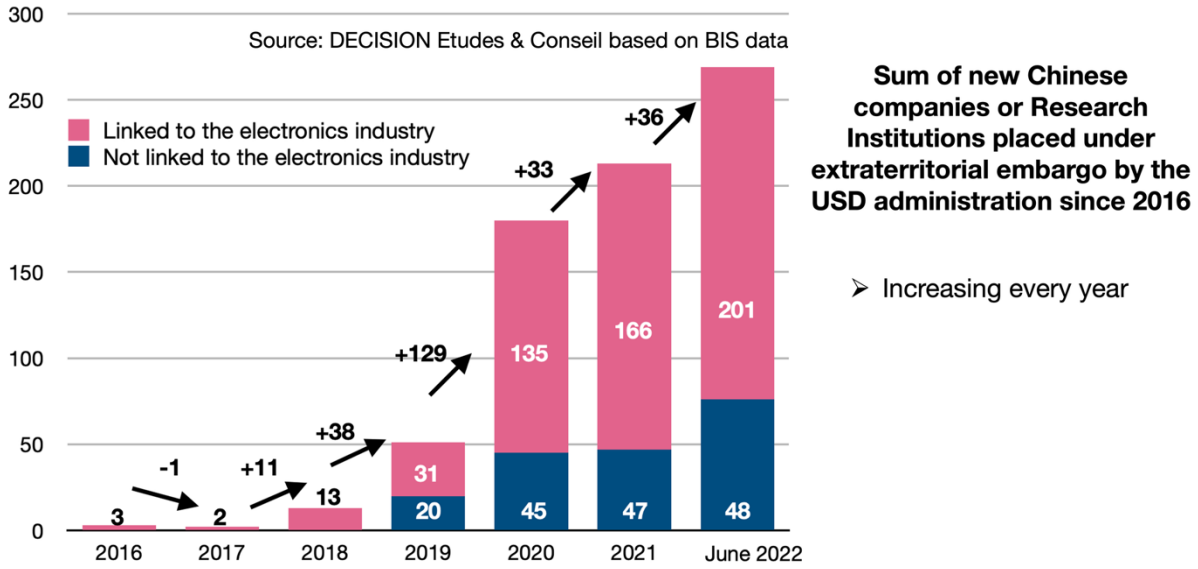
Figure 12: Summary of the export ban list on China from the US



Source: DECISION Etudes & Conseil based on BIS data

Introduced in 2020, the Foreign Direct Product Rule (FDPR) marked a significant extraterritorial expansion of U.S. export control jurisdiction. It applies to any foreign-made product that incorporates U.S. software, technology, or manufacturing equipment—regardless of where the item is produced. This provision became a cornerstone of Washington's efforts to prevent Chinese firms such as Huawei from accessing advanced chips and fabrication services abroad, including those provided by non-U.S. companies like TSMC.

Export controls have also been continuously tightened. Since 2022, updates to the Commerce Control List (CCL) and the Military End User (MEU) list have expanded restrictions to cover semiconductor manufacturing equipment, advanced computing chips, and supercomputing systems. These measures are no longer limited to individual firms but increasingly affect entire segments of the Chinese semiconductor ecosystem.

Deploying Industrial Policy to Secure Investment on U.S. Soil

In parallel with trade restrictions, the United States embraced industrial policy tools at a scale not seen in decades. The CHIPS and Science Act, along with the broader Inflation Reduction Act (IRA) of 2022, mobilized several hundred billion dollars in subsidies, tax credits, and public-private partnerships aimed at reshoring semiconductor manufacturing. Eligibility for support under these programs is explicitly tied to domestic content thresholds—ranging from 40% to 100% depending on the sector—thereby reinforcing the shift toward supply chain localization.

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From Selective Measures to Systemic Decoupling

The re-election of Donald Trump in 2025 marked a new acceleration of this momentum. U.S. policy shifted from selective restrictions toward a more systemic form of economic decoupling. In February 2025, a universal tariff of 10% on all Chinese imports was implemented, extending far beyond the scope of targeted semiconductor measures. A proposal for a 20% universal tariff is under discussion within the U.S. executive branch and could be adopted later in 2025.

This move was accompanied by a shift in diplomatic posture. The G7 Foreign Ministers' Communiqué of March 2025 omitted, for the first time, any reference to the "One China" policy—a signal of hardening positions on Taiwan. It also expressed unprecedented concern over China's expanding nuclear arsenal and military build-up, reinforcing the perception of China not only as a technological competitor but as a systemic geopolitical rival.

Taken together, these developments reflect a fundamental reordering of the U.S. approach to global trade. The objective is no longer simply to constrain China's access to cutting-edge technologies, but to rebuild a China-free value chain through a mix of domestic production, allied reshoring, and regulatory walls—an industrial strategy rooted in geopolitical logic.

2.3.3. China's Semiconductor Response to U.S. Sanctions

In response to escalating U.S. restrictions, China has intensified its push for technological autonomy in semiconductors. Its strategy rests on three pillars: long-term industrial planning, large-scale state support, and selective retaliation through the control of critical upstream resources.

A National Strategy of Technological Self-Reliance

Semiconductors have become a core focus of China's broader ambitions for national resilience.

The Dual Circulation Strategy, introduced in 2020, provides a long-term strategic framework for Chinese economic policy. It aims to rebalance growth by strengthening domestic consumption and insulating key sectors from foreign shocks.

This strategic orientation has been concretely translated into action through the 14th Five-Year Plan (2021–2025), which emphasizes technological self-sufficiency and identifies semiconductors, AI, and quantum computing as priority areas. The plan includes sustained increases in R&D investment—growing at 7% per year—and a

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regulatory push to replace imported technologies, especially for critical components and advanced manufacturing equipment. A notable example is the promotion of RISC-V, an open-source instruction set architecture that offers an alternative to Western-controlled platforms such as ARM and x86.

China's response also involves direct efforts to acquire foreign technologies. While China has been repeatedly blocked in its attempts to acquire key foreign semiconductor firms—such as Aixtron, Lattice Semiconductor, Lumileds—it has also managed to secure ownership stakes in others, notably Nexperia (via Wingtech Technology) and Imagination Technologies (via Chinese-backed investment through Canyon Bridge).

In parallel, China has intensified its efforts to attract foreign talent—particularly from Taiwan, which remains a key reservoir of expertise. Since 2018, over a thousand engineers have been recruited from the island, including more than 100 from TSMC alone. These efforts have focused increasingly on talent critical to the manufacturing of advanced processors. In 2017, SMIC appointed Liang Mong-Song, a former R&D Director at TSMC, as Co-CEO—marking a significant step in China's ambition to bridge its technology gap. In 2020, the now-defunct HSMC hired Chiang Shang-Yi, former CTO of TSMC, though he departed shortly after the project's collapse. More recently, Chinese firms have broadened their focus beyond Taiwan. In 2024, Huawei launched targeted recruitment campaigns aimed at engineers from ASML, Carl Zeiss, and Trumpf, seeking to build in-house capabilities in lithography and advanced optics. In January 2025, Hua Hong appointed Peng Bai as CEO. A veteran of Intel, he had spent 30 years at the company and served as VP of Logic Technology Development, overseeing the transition of leading-edge process nodes from research to mass production. These moves illustrate a consistent strategy: acquiring not just technology, but the human capital required to implement it at scale.

Massive Public Investment and Local Mobilization

Industrial policy has been reinforced by a renewed deployment of financial tools. The so-called Big Fund, China's National Integrated Circuit Industry Investment Fund, launched its second phase in 2019 with an allocation of $29 billion focused on equipment, design, and materials—following a first phase (2014–2019) of $22 billion largely dedicated to manufacturing. In 2024, a third phase was initiated, with $47 billion earmarked primarily for semiconductor manufacturing equipment, in response to tightening U.S. export controls.

In parallel, the Semiconductor Subsidy Plan (2022–2027) earmarks an additional $143 billion in public support, distributed through tax exemptions, capital grants, and direct loans.

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Fiscal incentives have also been expanded at the local level: under a 2020 central government directive, IC manufacturers at 28 nm and below are eligible for 10-year corporate tax holidays.

Local governments have become a key pillar of China's semiconductor funding ecosystem. Cities such as Shanghai, Shenzhen, Beijing, Wuhan, and Chengdu have significantly scaled up their own semiconductor investment funds. In many cases, provinces and municipalities are competing to attract semiconductor projects, offering land-use rights, R&D subsidies, and preferential loans far beyond what national programs provide.

These measures have helped stimulate the emergence of domestic suppliers in every segment of the value chain—from materials and equipment to design and OSAT.

Resource Weaponization and Strategic Retaliation

In addition to defensive measures, China has begun to weaponize its dominant position in the supply of critical raw materials. In July 2023, it imposed export licensing requirements on gallium and germanium, essential inputs for compound semiconductors. These were followed by a complete export ban on gallium, germanium, and antimony to the United States in December 2024. In February 2025, licensing requirements were further extended to include tungsten, tellurium, bismuth, indium, and molybdenum.

These decisions mark a shift in Beijing's strategy—from reactive compliance to active countermeasures. While China remains exposed to high-end technology sanctions, it is increasingly willing to exploit its own leverage points, particularly in upstream bottlenecks.

Strategic Partnerships and Global Outreach

Finally, China has stepped up its efforts to build selective international partnerships aimed at supporting its long-term semiconductor ambitions. While formal alliances remain limited, cooperation is expanding with countries in the Global South that offer complementary capabilities or strategic positioning. For example, China has deepened its engagement with Malaysia[5] through joint ventures and industrial cooperation in semiconductor assembly and packaging. It has also explored bilateral technology

[5] Penang hosts major Chinese and international OSAT facilities, and the Malaysian Investment Development Authority (MIDA) has facilitated several joint ventures involving Chinese firms such as JCET and Tongfu Microelectronics.

This project has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.

collaboration with countries like Brazil[6], particularly in microelectronics R&D. These targeted relationships reflect China's broader strategy to reduce exposure to U.S.-aligned supply chains and promote a more multipolar technological order.

2.4.Trade in Semiconductors Amid Geopolitical Fragmentation

Global trade—and semiconductor trade in particular—has been significantly shaped by the evolving geopolitical landscape. After more than two decades of uninterrupted growth, punctuated only by short-term contractions during the 2008 Subprime Crisis and the 2020 COVID-19 pandemic, both global trade and semiconductor trade began to plateau in 2024. This marks a clear inflection point in the organization of global value chains.

The impact of U.S.–China tensions is especially visible in bilateral semiconductor trade flows. Since 2018, the value of semiconductor-related exports and imports between the two countries has not only stagnated but declined, reflecting the cumulative effect of tariffs, export controls, and broader decoupling efforts. This decline is even more striking when compared to pre-2018 trends, which had shown robust annual growth.

In contrast, the European Union has maintained and even strengthened its semiconductor trade relations with both the United States and China. From 2018 to 2024, EU semiconductor exports to both partners have grown faster than the global average—reflecting the EU's dual positioning as both a trusted partner of the U.S. and a key supplier to the Chinese market.

As shown in Figure 13, the EU's trade balance across the semiconductor value chain has remained relatively stable over the past two decades, thanks to a structural trade surplus in semiconductor manufacturing equipment that offsets a consistent trade deficit in semiconductor products. In 2024, this surplus reached € 21.4 billion—driven primarily by exports of ASML equipment from the Netherlands to third countries—while the trade deficit in semiconductor products stood at € 10.8 billion, largely due to European back-end manufacturing facilities operating from Asia to supply the EU market.

Both imports and exports have surged since 2016, underscoring the EU's increasing reliance on third countries for both manufacturing and end-markets.

[6] Brazil has partnered with China in microelectronics through state-backed research institutions such as CEITEC and through bilateral cooperation frameworks under the Brazil–China High-Level Commission (COSBAN).

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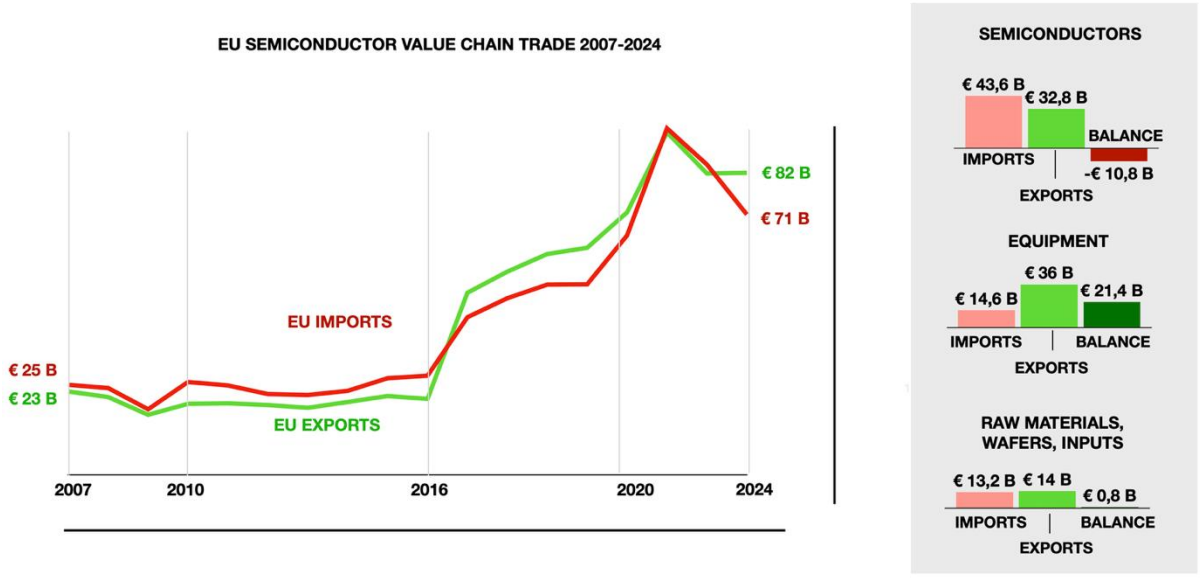
Figure 13: EU trade balance along the semiconductor value chain



Source: DECISION Etudes & Conseil

Figure 14 details the breakdown of EU trade by partner country, confirming the centrality of China and the U.S. In 2024, China was by far the EU's largest trading partner in semiconductors, with nearly € 30 billion in total trade volume and a trade surplus of € 3.4 billion for the EU. The United States ranked second with € 24 billion in trade volume and a surplus of € 1.7 billion, followed by Taiwan (€ 22 billion) with a deficit of € 1.6 billion. South Korea and Malaysia were tied in fourth position, each accounting for € 15 billion in trade volume. The EU recorded a € 1.5 billion deficit with South Korea and a significantly larger € 5.3 billion deficit with Malaysia—reflecting the strong presence of European manufacturing operations in the country that re-export to Europe. Japan ranked sixth with € 8.6 billion in trade volume and a trade deficit of € 4.1 billion for the EU.

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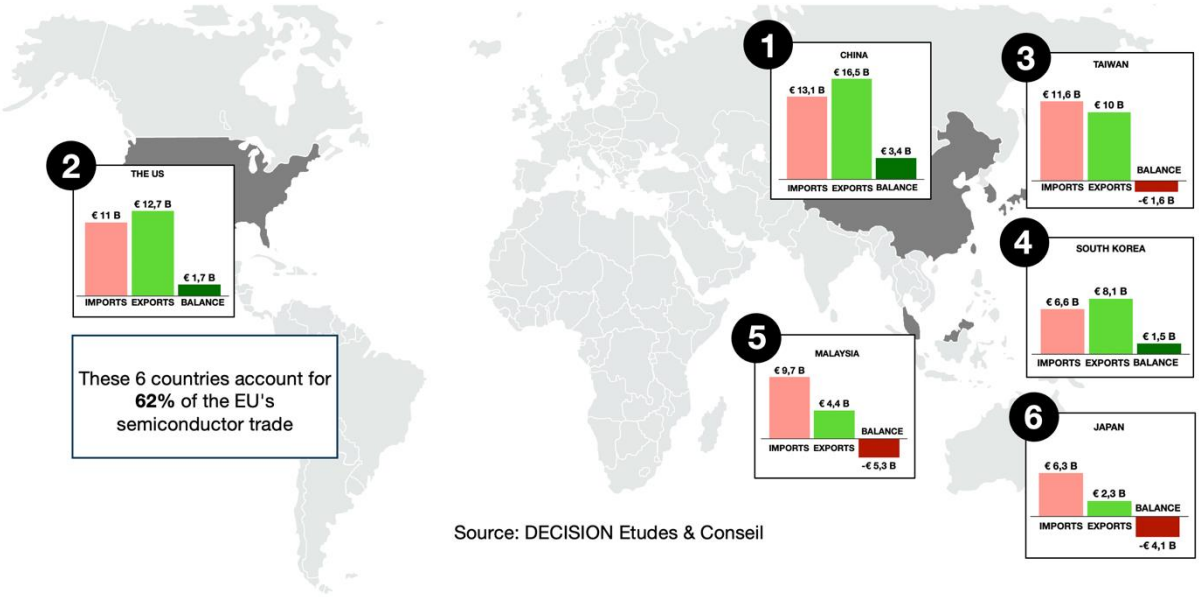
Figure 14: Main trading partners of the EU in semiconductors in 2024



Source: DECISION Etudes & Conseil

Taken together, these six countries account for 62% of the EU's total semiconductor trade.

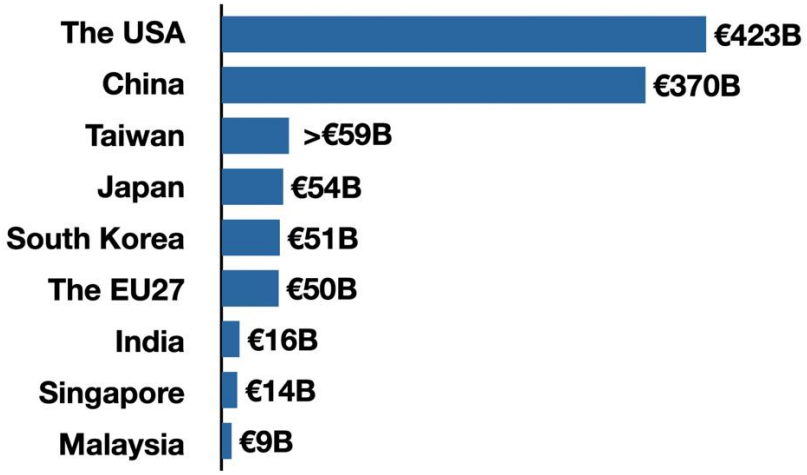
In a global context increasingly defined by decoupling and the emergence of bifurcated value chains—one gravitating toward the United States, the other toward China—the European Union must carefully navigate its position. Preserving and deepening commercial ties with both ecosystems is not just a matter of economic interest, but a strategic imperative to ensure supply chain resilience and safeguard Europe's technological autonomy.

This project has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.

3. Review of Semiconductor Investment Plans 2023-2025

The diagram below provides an overview of confirmed ongoing investments along the semiconductor value chain[7], by country or region, as of May 2025. Only individual projects exceeding € 1 billion are included.

Figure 15: Confirmed Semiconductor Investments Over € 1 Billion by Country/Region – May 2025



Source: DECISION Etudes & Conseil

Between 2024 and mid-2025, the global semiconductor investment landscape has entered a phase of consolidation, marked by regional disparities in momentum. While some countries continued to build on previous announcements, others saw a slowdown or reevaluation of key projects.

Not all regions experienced sustained investment growth since 2023. In the EU, several high-profile projects have been paused or cancelled—most notably Intel's € 30 billion fab in Germany and GlobalFoundries' withdrawal from the Crolles joint venture in France—bringing into question the reliability of foreign-led investments in Europe. Despite this, new initiatives such as Silicon Box's advanced packaging facility in Italy and Broadcom's back-end project in Spain have diversified the EU's semiconductor footprint. Japan similarly saw slower momentum, with delays in projects from Kioxia, Renesas, and Sony, and the cancellation of a planned foundry by PSMC and SBI. Singapore and Malaysia experienced fewer new announcements, and in Malaysia, reports suggest that Intel's major advanced packaging investment may be on indefinite hold.

[7] Considering semiconductor manufacturing, design, EDA & IP, RTOs & Pilot Lines, Equipment, Materials & Tools.

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By contrast, several countries maintained or intensified their investment pace. India saw its semiconductor strategy begin to materialize, with six confirmed manufacturing investments (five in back-end, one in front-end) receiving government support. The US consolidated its position as a global semiconductor powerhouse with large-scale expansions from Intel, Micron, Samsung, and TSMC -whose investment in Arizona now exceeds € 150 billion. Taiwan has seen continued dominance by TSMC, which is expanding capacity for nodes below 3nm while also investing in advanced packaging. China, despite export controls, remains the world's leading spender on semiconductor equipment8 and continues to drive vertically integrated investments across the value chain, notably supported by the new €44 billion Big Fund III.

Across leading regions, there is a clear shift toward building advanced front-end manufacturing capacity, particularly for nodes below 3nm (as seen in the US, Taiwan, and South Korea). Simultaneously, several governments are prioritizing advanced packaging and domestic design capabilities to move further upstream in the value chain. Malaysia's partnership with ARM and Singapore's NSTIC initiative illustrate such efforts.

3.1. The EU

The map below provides an overview of the main semiconductor investments announced at the finalization stage of the EU CHIPS Act (2023), and covering the 2022–2030 period[9].

[8] According to SEMI.
[9] Only investments exceeding €1 billion are considered in this analysis.

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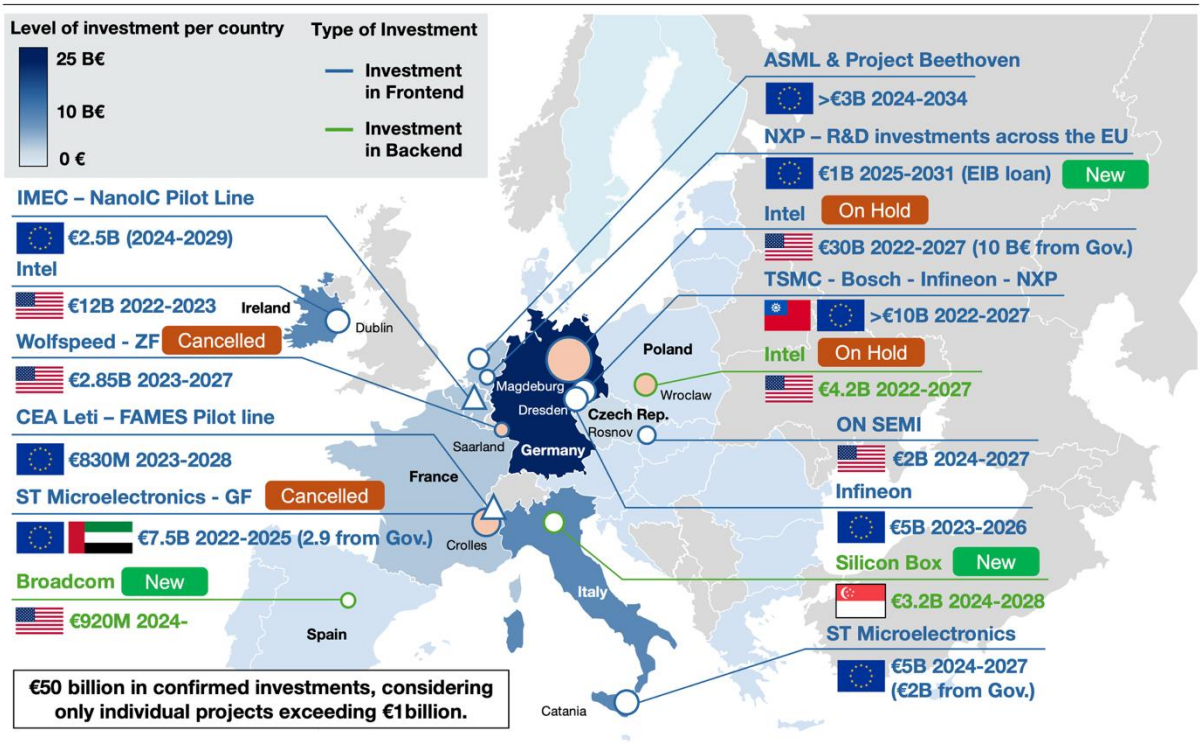
Figure 16: Evolution of Semiconductor Investment Plans in the EU (Over € 1B), January 2024 – May 2025



Source: DECISION Etudes & Conseil

These include:

- Intel's € 12 billion expansion in Leixlip (Ireland) to produce 7nm chips.
- The creation of European Semiconductor Manufacturing Company (ESMC) -a joint venture led by TSMC with Bosch, NXP, and Infineon in Dresden (Germany) for 300mm wafer production using 12nm nodes, with a total investment exceeding € 10 billion and 40% expected in public support.
- STMicroelectronics' € 7.5 billion co-investment in Crolles (France), with GlobalFoundries to produce 22nm and 18nm FD-SOI chips, supported by € 2.9 billion in state aid.
- Infineon's building of a € 5 billion chip plant in Dresden (Germany), for 12nm power semiconductors and analog/mixed-signal devices, with € 1 billion in subsidies.

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- STMicroelectronics' € 5 billion investment for a new megafab in Catania (Italy), focused on silicon carbide devices, complemented by a € 730 million investment in a SiC substrate manufacturing facility on the same site.

- Bosch's € 3 billion investment plan in Germany by 2026 to strengthen its semiconductor operations. The investment includes expanding cleanroom capacity at its Dresden site, establishing new R&D centers in both Dresden and Reutlingen, and allocating over € 570 million specifically for infrastructure-related upgrades -all within the € 3 billion total.

- More than € 3 billion is being invested in the Netherlands to strengthen the Brainport ecosystem and support ASML's continued growth. This includes approximately € 2.5 billion (2024–2030) in public investment under 'Project Beethoven'—a regional initiative involving national and local governments, ASML, and other high-tech companies—to upgrade infrastructure, housing, energy, and education. ASML is contributing directly as well, notably through an € 80 million (2024–2034) investment in a joint cleanroom with Eindhoven University of Technology, and through phased expansions of its Veldhoven and Eindhoven campuses—near the airport—including a 357,000 m² facility designed to ultimately accommodate 20,000 additional employees, with the first staff arriving in 2028 and full build-out expected from 2030.

Since 2024, several of the most emblematic previously announced investments have been revised, postponed, or cancelled. Among the most notable updates:

- Intel has durably put on hold its two flagship projects in the EU: the € 30 billion foundry in Magdeburg, Germany, and the € 4.6 billion assembly and test facility near Wrocław, Poland. These projects have been delayed for at least two years amid financial losses and global cost-cutting measures by the company.

- Similarly, GlobalFoundries has withdrawn from its planned € 7.5 billion joint fab project in Crolles, France, leaving STMicroelectronics to reconsider the scope of the investment.

- Wolfspeed, in partnership with ZF, has also cancelled its planned € 2.85 billion silicon carbide fab in Ensdorf, Germany, citing weak market demand and uncertainty, with ZF announcing its intent to exit the venture[10].

In parallel, new investment projects have been announced across the continent:

[10] Wolfspeed faces serious financial difficulties and is preparing to file for bankruptcy.

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- In Italy, Silicon Box revealed a € 3.2 billion plan to establish an advanced semiconductor packaging and testing facility in Novara, Piedmont. The project, supported by € 1.3 billion in approved state aid, is expected to generate 1,600 highly skilled jobs and contribute to building Europe's back-end capabilities.
- In Spain, Broadcom confirmed a nearly €1 billion investment to develop a large-scale back-end semiconductor facility.
- NXP secured a € 1 billion EIB loan in January 2025 to fund semiconductor R&D in Austria, France, Germany, the Netherlands, and Romania through 2026, with a six-year repayment period (until 2031).

Among the investments that fall below the €1 billion threshold and thus do not appear in the figure below, several smaller but strategic investments have also been announced since early 2024:

- Analog Devices announced in 2023 a € 630 million in a new R&D and manufacturing facility in Limerick, Ireland, to triple its European wafer production capacity and create 600 high-skilled jobs, under the IPCEI framework.
- In Austria, AMS-OSRAM has announced a €588 million investment plan to expand its chip production capacity at its Premstätten site by 2030, including a foundry activity, with € 200 million in public funding requested under the European CHIPS Act. The project is expected to create around 250 new jobs.
- AT&S invested €500 million in its Leoben (Austria) site to build a state-of-the-art competence center for IC substrate R&D and small-series production, with construction from 2022 to 2025 and an expected additional workforce of ~700 specialists.
- Global Wafers has committed to establishing a new 300mm wafer production facility in Italy, supported by national and European funding, to strengthen the regional supply of silicon wafers.
- Meanwhile, Vishay is also investing in production capacity in Germany and the Czech Republic, aiming to strengthen European supply chains for passive components.

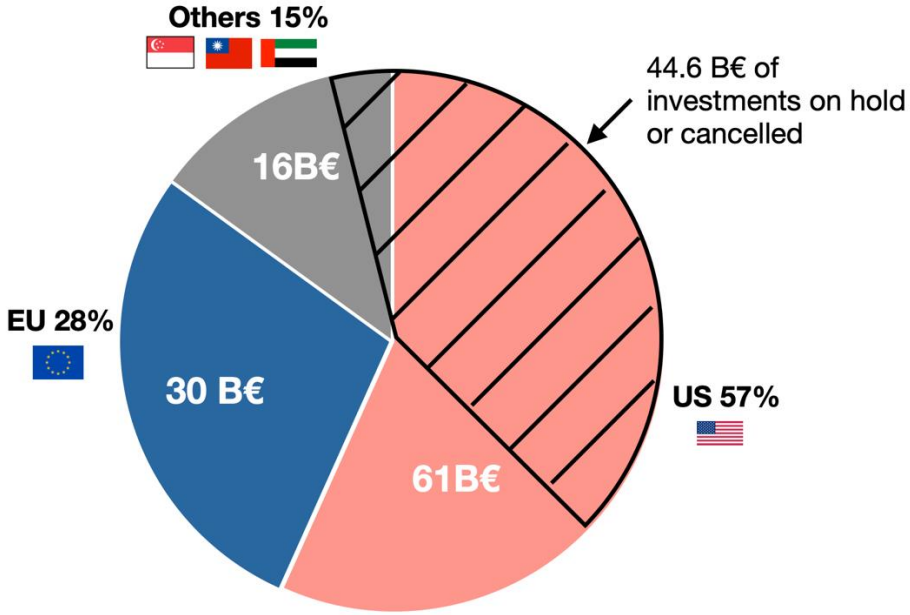
Beyond the major investments exceeding € 1 billion, the pie chart below shows the distribution of total capital expenditures from semiconductor projects announced in the EU since the launch of the EU CHIPS Act, covering the period up to their expected production start dates.

This project has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.

As of 2025, total investments under the EU CHIPS Act amount to approximately € 108 billion. However, this total includes several major projects that have since been put on hold, which are identified in the chart with a hatched pattern. These suspended investments amount to € 44.6 billion, primarily stemming from US companies, and corresponding to 42% of the total announcement associated with the EU CHIPS Act.

As a result, total confirmed investments under the EU CHIPS Act in 2025 amount to € 63 billion.

Figure 17: Total semiconductor investments under the EU CHIPS Act (2022-2027), breakdown by nationality of beneficiaries



Source: DECISION Etudes & Conseil

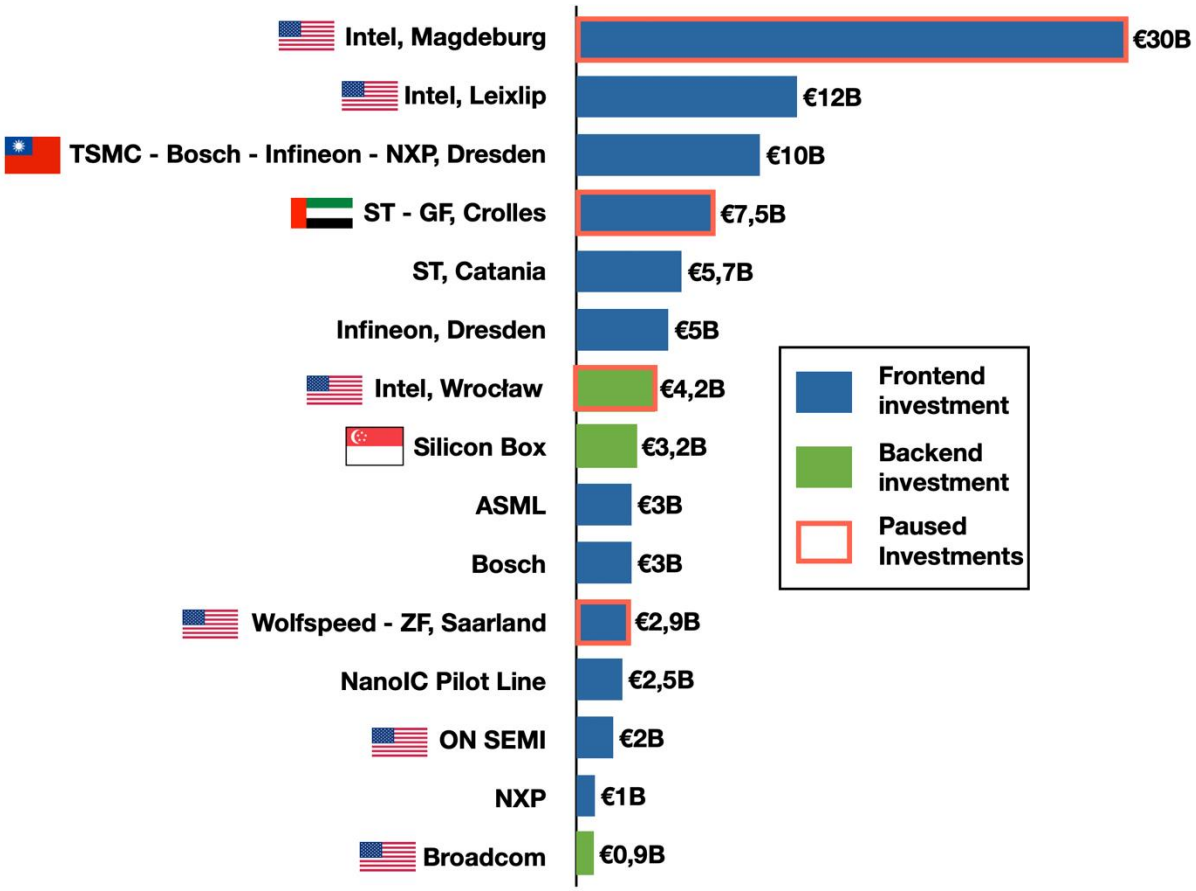
In terms of investment origin, US companies account for € 61 billion, or 57% of the total, when including both active and paused projects. This is followed by EU-based companies, which represent € 30 billion, or 28% of the total. The remaining € 16 billion (15%) originates from companies headquartered in other regions, including Taiwan (TSMC), Singapore (Silicon Box) and the United Arab Emirates (GlobalFoundries).

The EU stands out as the only region whose CHIPS Act has been dominated by foreign investment -accounting for 72%, including 57% from a single third country (the US)- while all cancelled projects so far have precisely involved US companies.

This project has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.

While cancelling its investment in Crolles (France), GlobalFoundries confirmed in June 2025 $ 16 billion investment in the US. An additional $ 1.1 billion investment is also under consideration for its plant in Dresden (Germany).

Figure 18: TOP 15 semiconductor investments in the EU from 2022 to 2034



Source: DECISION Études & Conseil

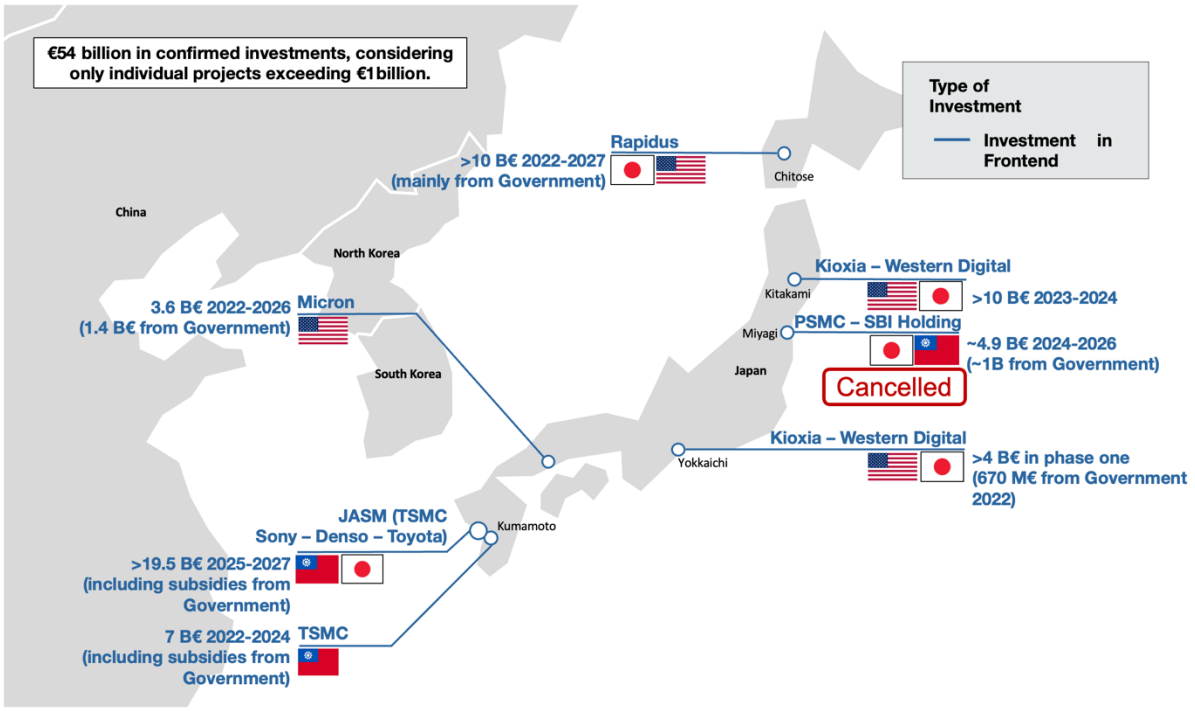
This project has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.

3.2.Japan

Confirmed ongoing semiconductor investments in Japan now amount to € 54 billion, considering only individual projects exceeding € 1 billion. An amount roughly equivalent to semiconductor investments in the EU.

However, most of these investments were already planned in 2023.

Figure 19: Ongoing major investments in Japan, May 2025



Source: DECISION Etudes & Conseil

The most emblematic initiative remains Rapidus, Japan's flagship project to regain leadership in advanced semiconductor manufacturing. Backed by eight major Japanese corporations (Denso, Kioxia, MUFG Bank, NEC, NTT, SoftBank, Sony, and Toyota), Rapidus was launched in 2022 with an initial private sector contribution of € 44.6 million. Since then, the Japanese government has significantly expanded its support, committing over € 4.9 billion as of March 2025, part of a broader national effort to allocate more than € 61 billion by 2030 to support semiconductor and AI development. Rapidus is targeting mass production of 2nm chips by 2027, with pilot line testing launched in April 2025. The Hokkaido facility is progressing, and Rapidus is actively courting partnerships with major global clients, including Apple and Google.

This project has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.

TSMC has also reinforced its presence in Japan through its subsidiary JASM (Japan Advanced Semiconductor Manufacturing), a joint venture with Sony, Denso, and Toyota. Mass production at the first Kumamoto fab began in December 2024, though the plant is not yet operating at full capacity. A second fab, originally scheduled to begin construction in fiscal year 2024, has been delayed but is still expected to start production by 2027. These fabs cover a wide range of nodes (22/28nm and 12/16nm for the first, down to 6nm for the second), supplying key Japanese customers in both embedded and stand-alone user industries (automotive, consumer audio & video…).

Kioxia completed construction of its Fab2 facility in Kitakami in July 2024, aiming to expand its flash memory production capabilities. However, the company has postponed mass production, now expected in late 2025 or beyond, depending on market recovery.

Micron continues to implement its plans for up to € 3.6 billion investment in EUV-based DRAM production in Hiroshima, with governmental support.

Finally, Shin-Etsu Chemical also announced a € 507 million investment in April 2024 for a new facility in Gunma Prefecture, set to manufacture lithography materials with initial operations beginning in 2026.

However, not all planned investments have materialized as expected. In April 2024, the joint venture between Powerchip Semiconductor Manufacturing Corp (PSMC) and SBI Holdings to build a foundry in Miyagi Prefecture was cancelled. PSMC cited unwillingness to assume project risks, while SBI expressed intent to seek new partners. The project had originally planned a € 4.9 billion investment, aiming for 2027 production focused on automotive semiconductors.

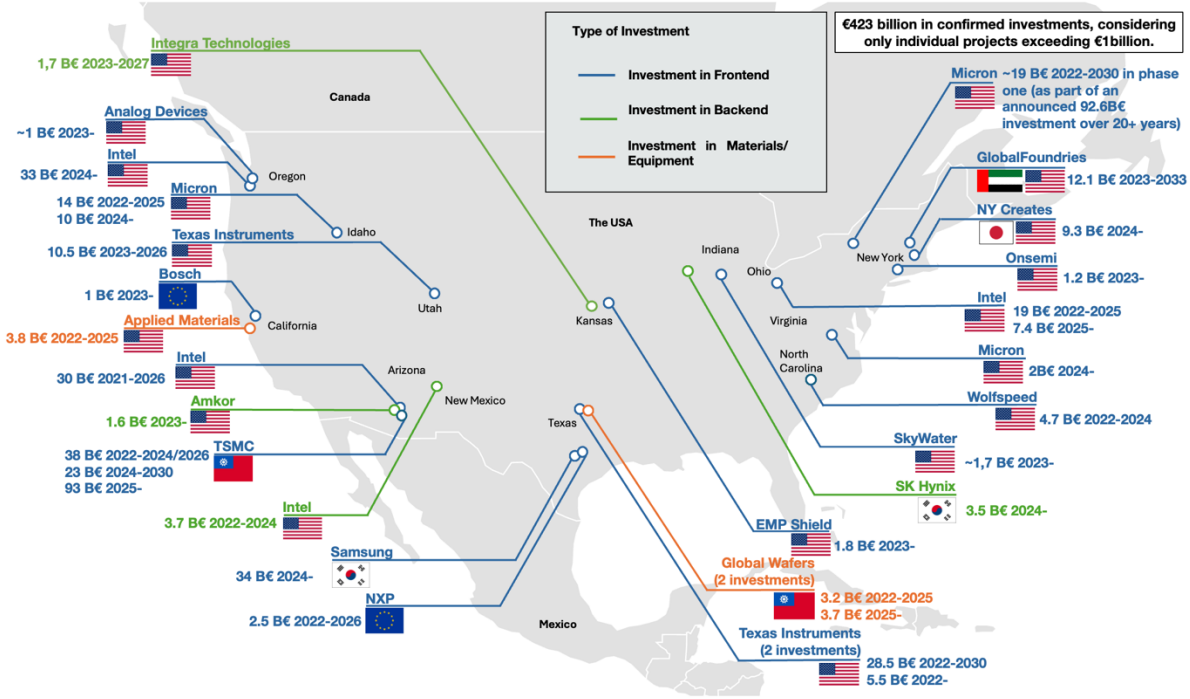
Other domestic players have faced delays. Renesas reopened its Kofu plant in April 2024 after a nine-year hiatus, but postponed mass production due to weak demand for power semiconductors. Rohm, which acquired a new facility in 2023, began pilot runs in late 2024 but has not confirmed the start of volume production. Sony's new wafer plant in Isahaya, while operational, is expanding cautiously due to sluggish demand for image sensors.

This project has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.

3.3.The USA

Confirmed ongoing semiconductor investments in the US now amount to € 423 billion, considering only individual projects exceeding € 1 billion. This impressive figure reflects a substantial surge between early 2024 and 2025. This represents a level of investment 8 to 9 times higher than that of the EU during the same timeframe.

Figure 20: Ongoing major investments in the US, May 2025



Source: DECISION Etudes & Conseil

TSMC, the Taiwanese leader in the global foundry segment, is currently the largest investor in the semiconductor industry. Its Arizona-based project has grown from an initial € 38 billion to € 61 billion and ultimately reached a total commitment of € 153 billion as announced in March 2025. This investment spans the entire value chain, including six leading-edge fabrication plants covering TSMC's most advanced process nodes -N5, N4, and N3 (FinFET), as well as N2 and A16 (nanosheet technologies)- alongside two advanced packaging facilities and a major R&D center. The first fab began 4nm production in late 2024, with subsequent phases scheduled through the end of the decade. The project is backed by up to € 6.1 billion in CHIPS Act funding and € 4.6 billion in federal loans. Nonetheless, TSMC has flagged potential risks to the project's long-term viability due to proposed US tariffs on chips produced in Taiwan, highlighting the political sensitivities tied to such large-scale foreign investment.

This project has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.

Intel announced substantial increases in its investments: an additional € 7.4 billion in New Albany, Ohio (totaling € 26 billion); a new € 33 billion commitment in Hillsboro, Oregon; and an increase from € 18.5 billion to € 29.6 billion in Arizona. These projects are supported by up to € 7.2 billion in federal funding through the CHIPS Act.

GlobalFoundries unveiled a new € 12.1 billion plan over the next decade to expand its Malta, New York, facility, with € 1.3 billion in CHIPS Act incentives.

Micron secured € 5.7 billion in federal funding for its megafab project in Clay, New York, marking the largest memory manufacturing investment in US history.

Additionally, NY CREATES announced a € 9.3 billion public-private partnership to establish a new R&D center at the Albany Nanotech Complex.

In parallel, Samsung confirmed a € 34 billion expansion plan in Texas, covering two additional leading-edge fabs, a new R&D center, and upgrades to its Austin facility, all expected to be operational by 2030, with up to € 5.9 billion in CHIPS Act support.

The back-end segment has also seen notable investments within the same time.

- Amkor is advancing its € 1.6 billion advanced packaging and test facility in Peoria, Arizona, supported by € 377 million in CHIPS Act funding.
- Intel confirmed in late 2023 the extension of its advanced packaging operations in New Mexico by expanding Fab 9 into the adjacent Fab 11x, with the project formally integrated into the CHIPS Act investment portfolio in 2024.
- Furthermore, in April 2024, SK Hynix entered into an agreement with the State of Indiana to invest in advanced chip packaging, highlighting the growing involvement of international firms in this segment.

The US also benefits from investments upstream in the supply chain: GlobalWafers completed a € 3.2 billion facility in Sherman, Texas, and announced an additional € 3.7 billion investment in May 2025 to expand production at the site. This expansion aims to enhance domestic supply of high-purity silicon wafers, a critical component for semiconductor manufacturing.

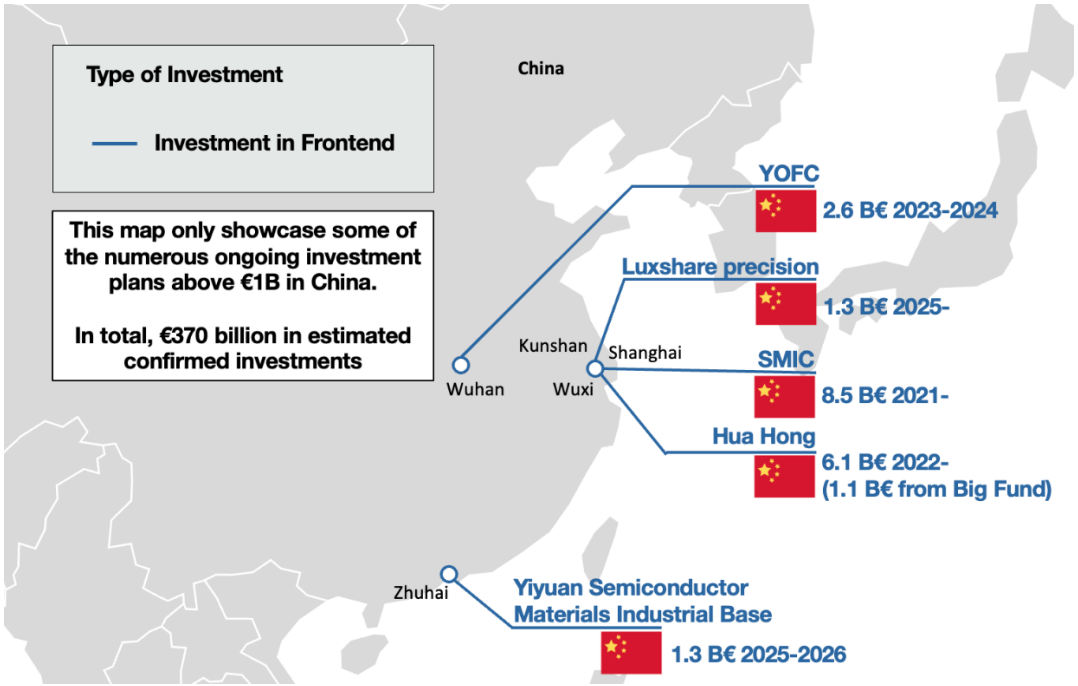
This project has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.

3.4.China

China stands out as one of the world's top investors in semiconductors, alongside the US. The main investment projects described below are also featured on the accompanying map. While the map provides a useful overview of China's current investment landscape on investments amounting for € 1 billion and above, it is not exhaustive. Unlike large public investment programs or regulatory disclosures by listed companies, many private-sector investments in China are not systematically announced or publicly reported. As a result, some relevant projects currently underway may not appear despite their significance. DECISION estimates that the total volume of ongoing, confirmed public and private investment plans across the semiconductor value chain in China ranges between € 370 billion and € 500 billion — a level comparable to that of the United States.

China is undergoing a renewed phase of investment in its semiconductor sector, marked by the launch of the third phase of its National Integrated Circuit Industry Investment Fund, known as "Big Fund III," in mid-2024. With a total capital of € 44 billion -the largest to date- this fund is supported by major state-owned banks such as ICBC and China Construction Bank. Big Fund III reflects Beijing's strategic ambition to reach self-sufficiency in semiconductors and become a global leader in advanced technologies such as AI, 5G, and quantum computing by 2030. The fund is directed toward manufacturing, equipment, materials, and design.

Figure 21: Ongoing major investments in China, May 2025



Source: DECISION Etudes & Conseil

Despite facing international export controls, China is expected to remain the world's leading spender on semiconductor equipment in 2025, with a projected € 35 billion in investment. This amount, although down from € 46.3 billion in 2024, still far exceeds spending of other countries. Domestic equipment makers such as NAURA, AMEC, and Huawei-affiliated SiCarrier are growing rapidly and benefiting from policy support. These firms are aiming to challenge foreign incumbents across lithography, etch, and metrology segments.

The second phase of Big Fund has continued investing in upstream segments, targeting equipment and material producers, as well as EDA tool developers and chip design firms. It notably funded Chongqing XLMEC, a specialty fab focused on automotive-grade chips, and co-founded Jinke Silicon Material in Taiyuan to boost domestic 300mm silicon wafer production.

China's leading foundries, SMIC and Hua Hong, are pressing forward with capacity expansion. SMIC plans to invest approximately € 7 billion in 2025 and aims to add one new fab each year, targeting 50,000 12-inch wafers per month. The company is also scaling its automotive-grade chip production, which could represent up to 10% of its revenue. Hua Hong, meanwhile, is advancing into 28nm and 22nm nodes and is expanding its Wuxi fab to reach 20,000 wafers per month by late 2025.

Several large-scale projects also advanced in 2025:

- In Zhuhai, the Yiyuan Semiconductor Materials Industrial Base broke ground, with an investment of € 1.3 billion to produce synthetic quartz and SiC power substrates.
- In Kunshan, Luxshare Precision is investing € 1.5 billion in a smart terminal and acoustic components industrial park.
- Wuhan's YOFC is ramping up production of SiC wafers and power device modules, since its opening in 2024 backed by € 2.6 billion in investment.

Beijing is positioning itself as a rising semiconductor hub. In late 2024, a € 4.2 billion investment initiative was launched to build a 12-inch wafer fab led by Yandong Microelectronics and BOE Technology. The facility aims to reach 370,000 wafers per month by 2027 and bridge the gap with the Yangtze River Delta region.

China is also reinforcing its packaging capabilities. JCET is investing around ~€ 560 million in its flagship advanced packaging plant for automotive chips in Shanghai's Lingang area. Construction began in August 2023, and the facility is expected to be completed and operational by mid-2025, covering 200,000 m² to support China's

This project has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.

rapidly growing EV semiconductor market. In parallel, JCET has acquired 80% of SanDisk Semiconductor Shanghai from Western Digital for € 580 million, signaling a strategic push into the storage packaging market. This move is aligned with the global surge in demand for NAND flash memory and supports JCET's ambition to become a leading player in advanced memory packaging.

Despite growing geopolitical and supply chain tensions, Samsung announced in early 2025 the upgrade of its Xi'an NAND flash production facility by transitioning to a 286-layer (V9) process technology, following earlier reports of reduced output due to weak demand. No official investment amount was disclosed.

SK Hynix, on the contrary, took steps to restructure its presence in China. The company announced the sale of nearly 50% of its Wuxi-based foundry subsidiary to the Wuxi Industry Development Group, a Chinese state-owned enterprise. The transaction includes a 21.3% stake sold for € 151 million and the transfer of intangible assets, including process technologies, valued at € 91 million. Additionally, the Chinese group is set to acquire another 28.6% stake through a capital increase, giving it majority control. SK Hynix described the decision as part of its long-term strategy to optimize its business structure and pursue new growth opportunities.

3.5.Taiwan

In Taiwan, the investment landscape for semiconductors has gained renewed momentum in 2025, building on previously announced projects expected to begin production this year while adding major new commitments by both local and international players.

Confirmed ongoing semiconductor investments Taiwan amount to € 59 billion, considering only individual projects exceeding € 1 billion and including only TSMC's investment for 2025. This represents a level of investment significantly higher than that of the EU over the same period.

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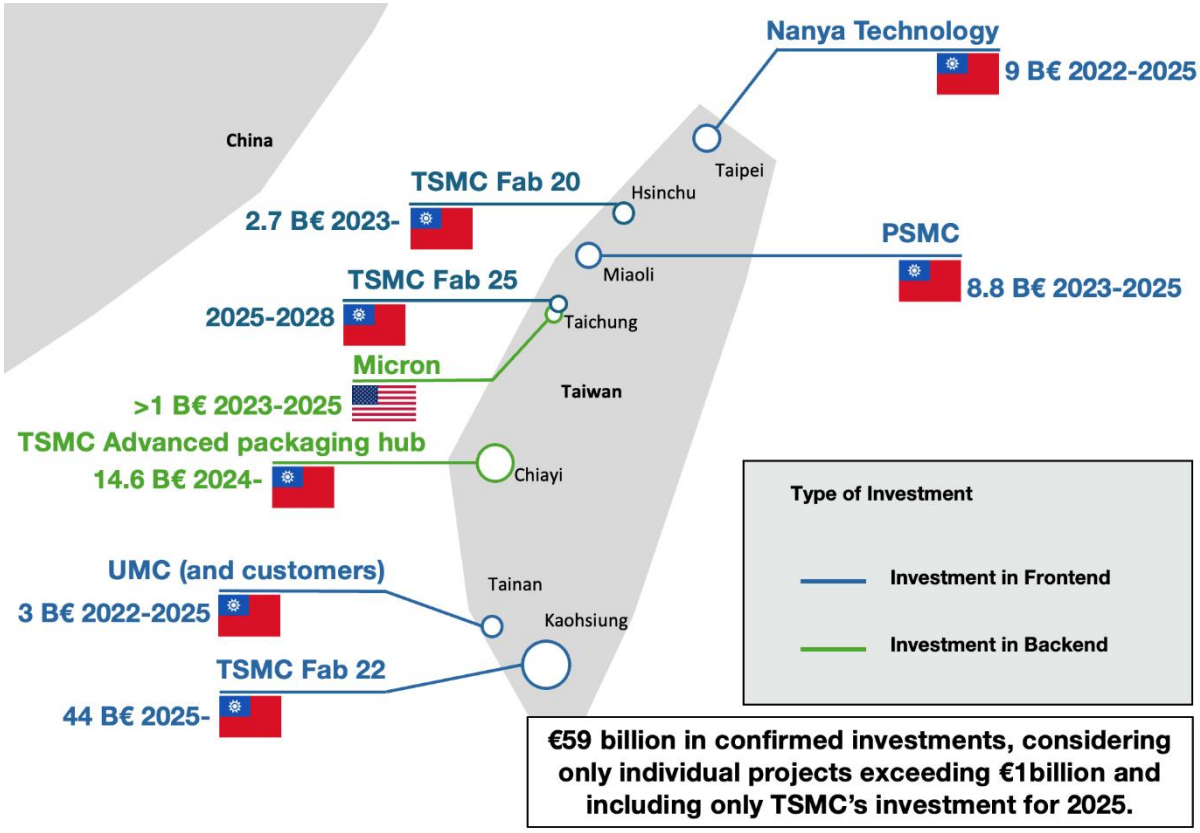
Figure 22: Ongoing major investment in Taiwan, May 2025



Source: DECISION Etudes & Conseil

Several large-scale projects announced earlier are expected to begin production in the second half of 2025. These include:

- TSMC's Fab 20 (Phase 1) in Hsinchu and Fab 22 (Phase 1) in Kaohsiung, both designed for 2nm process manufacturing, are currently being equipped and ramped up.
- Nanya's € 9 billion (NT$300 billion) investment in Taiwan for the 2021–2025 period—dedicated to building a new 12-inch DRAM fab in New Taipei City's Taishan district—is progressing on schedule. Construction began in 2022, and the facility is expected to begin production in 2025, with a planned capacity of 45,000 wafers per month, supported in part by customer prepayments.
- Powerchip Semiconductor Manufacturing Corporation (PSMC) officially inaugurated its new 12-inch Tongluo Fab in Miaoli in May 2025. With over € 2.3 billion invested to date out of a projected € 8.8 billion total, the facility has begun trial production and will serve as a platform to attract international clients and advance PSMC's process technologies.

This project has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.

- UMC € 3 billion (NT$100 billion) investment in Taiwan for the 2021–2025 period, aimed at expanding 300 mm wafer production -particularly at its Fab 12A P6 site in Tainan- is on track to be completed by the end of 2025. The investment includes infrastructure and equipment, supported in part by customer prepayments to secure long-term capacity.
- Micron is expanding production in Taiwan, ramping up HBM3E and 1β node production in 2025, and introducing the 1γ node using EUV at its Taichung facility, which also serves as the initial packaging site for HBM3E.

Meanwhile, TSMC has reaffirmed its long-term commitment to domestic operations. In 2025 alone, it plans to build eight wafer fabs and one advanced packaging plant, reflecting a capital expenditure of € 35 to € 39 billion.

Among these new developments:

- Construction began on Fab 25 in Taichung, expected to produce chips on the future A14 (1.4nm-class) process technology starting in 2028.
- Beyond its phase 1, in Kaohsiung, the Fab 22 complex is progressing through its five-phase development, with:
    - Phase II topped out
    - Phase III under construction
    - Phases IV and V announced
- In Chiayi, TSMC is building a new advanced packaging hub, comprising six planned plants and more than € 14.6 billion in investment. While construction began in April 2025 for the additional facilities, equipment installation for the previously announced AP7 plant was delayed from Q3 to Q4 following safety incidents. The site will expand CoWoS packaging capacity, critical to high-performance chips like NVIDIA's B100.

At its 2025 North America Technology Symposium, TSMC also revealed its roadmap for A14, a 1.4nm-class node based on second-generation GAA nanosheet transistors and NanoFlex Pro technology. Mass production is targeted for 2028, with a version featuring backside power delivery scheduled for 2029.

Taiwan stands out as one of the few countries -along with China and South Korea- where semiconductor investments are driven almost exclusively by domestic firms. Except for Micron, all major projects are led by Taiwanese companies, particularly TSMC. These investments are primarily directed toward increasing front-end capacity at advanced nodes below 3nm, positioning Taiwan at the forefront of cutting-edge chip

This project has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.

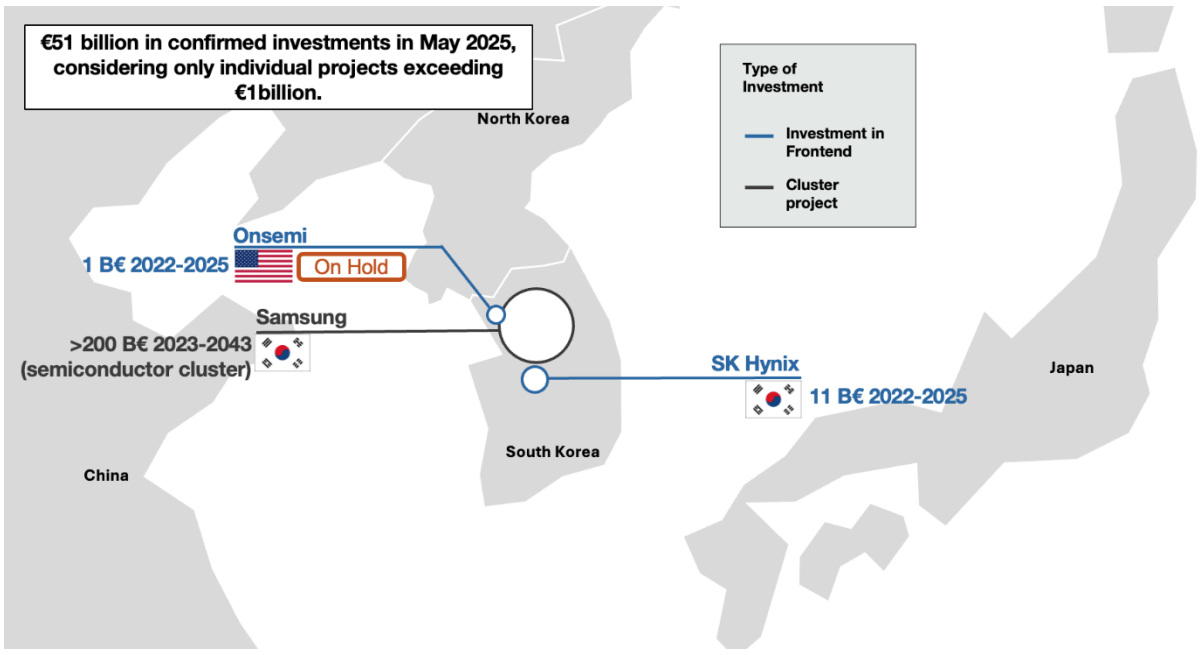
production. At the same time, TSMC is balancing this front-end expansion with significant investments in advanced packaging, notably through the development of its new packaging hub in Chiayi.

3.6.South Korea

Confirmed ongoing semiconductor investments in South Korea amount to € 51 billion, considering only individual projects exceeding € 1 billion [11]. An amount roughly equivalent to semiconductor investments in the EU.

In South Korea, semiconductor investments have intensified through a combination of large-scale private projects and expanded public support. The government has increased its financial commitment to the sector, raising its investment plan from € 17.6 billion to € 22.4 billion.

Figure 23: Ongoing major investments in South Korea, May 2025



Source: DECISION Etudes & Conseil

The most significant private-sector project is Samsung Electronics' more than € 200 billion (₩300 trillion) plan to create the world's largest high-tech semiconductor manufacturing cluster in Gyeonggi Province over the next 20 years (2023-2043). The

[11] Only half of Samsung's planned investment is considered, in order to cover the period 2023-2033 and enable comparison with other countries and regions. In other words, the €100B planned investment over the 2033-2043 period are excluded.

This project has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.

cluster will consist of five fabs producing memory and logic chips and is expected to attract up to 150 related companies. This mega-cluster is a core component of the government's ambition to create a globally competitive semiconductor ecosystem and incentivize broader industrial investments. However, out of the € 200 billion planned investment by 2043, only 20% is currently committed, amounting to € 40 billion.

In parallel, SK Hynix has greenlit a € 6.4 billion investment to construct the first of four planned fabs in the Yongin Semiconductor Cluster. Construction of the first fab began in March 2025 and is slated for completion by May 2027. The Yongin site, spanning over 4 million square meters, is envisioned as a global production hub for next-generation AI memory semiconductors. The broader cluster will include a semiconductor cooperation complex involving more than 50 local companies.

By contrast, ON SEMI has halted its planned € 1 billion investment in Bucheon. In 2025, the US firm halted expansion of its silicon carbide (SiC) power management IC facility, citing a sharp decline in South Korean EV sales and weaker-than-expected demand. Most of its engineers were recalled to the US, and research staff remaining on-site are expected to be reassigned.

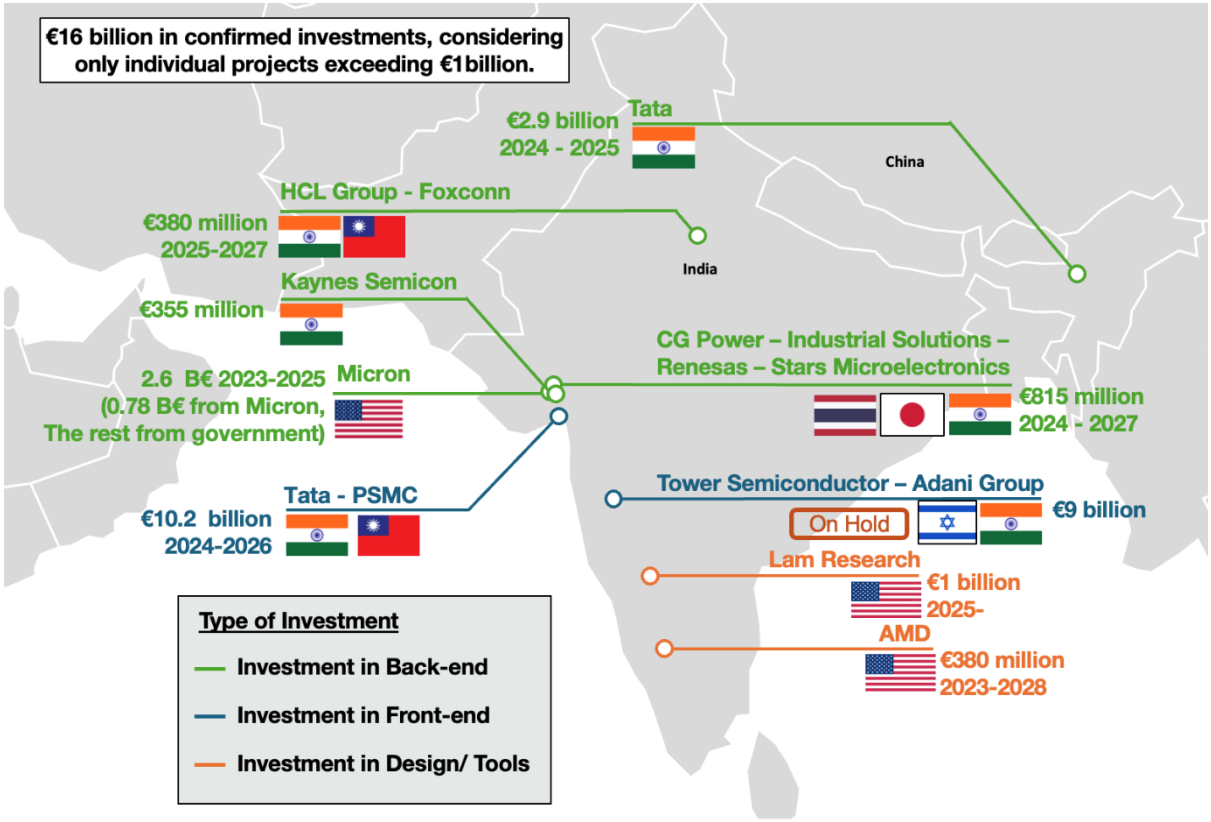
3.7.India

Between late 2023 and mid-2025, the semiconductor investment landscape in India has significantly matured. From a single confirmed project in 2023, the country now hosts six manufacturing investments that have received official approval and government support. These investments are part of India's broader strategy to strengthen domestic chip production under the India Semiconductor Mission, which provides subsidies for both front-end and back-end manufacturing.

Confirmed ongoing semiconductor investments in India amount to € 16 billion, considering only individual projects exceeding € 1 billion. This represents a level of investment 3 times lower than that of the EU over the same period, and roughly equivalent to semiconductor investments in Germany.

This project has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.

Figure 24: Current state of major semiconductor investments in India, May 2025



Source: DECISION Etudes & Conseil

Five of the six confirmed projects focus on back-end (OSAT) manufacturing:

- Tata Electronics is developing a back-end facility in Marigaon, Assam with a € 2.9 billion investment, expected to commence operations in 2025.
- Micron remains one of the earliest confirmed investments, with a chip packaging and testing plant in Sanand, Gujarat. Initially slated for completion in 2024, the project has experienced delays and is now expected to become operational late 2025. The investment totals € 2.6 billion, with € 780 million from Micron and the remainder from central and state subsidies.
- CG Power – Industrial Solutions – Renesas – Stars Microelectronics formed a joint venture for an OSAT plant in Sanand, Gujarat. Approved under India's semiconductor scheme in February 2024, the project involves a € 815 million investment over five years. It will ramp up to a daily capacity of 15 million units and manufacture both legacy and advanced packages (QFN, QFP, FC BGA, FC

This project has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.

CSP). CG Power holds 92.3% of the venture, with Renesas and Stars Microelectronics contributing the rest.

- HCL Group and Foxconn announced a joint OSAT venture in May 2025, with a planned investment of € 380 million. Located in Uttar Pradesh near Jewar airport, the plant will produce 36 million display driver chips annually, with commercial production expected by 2027.

- Kaynes Semicon is set to become the first Indian firm to deliver a packaged chip, with production scheduled to begin in July 2025. Backed by a government-approved investment of € 355 million, the facility in Sanand will have capacity for 6.3 million chips per day. Initial output is already committed to U.S.-based Alpha Omega Semiconductor.

The only confirmed front-end project is the Tata Electronics – PSMC (Taiwan) partnership to establish India's first wafer fabrication facility in Dholera, Gujarat. Signed in September 2024, the € 10.2 billion project is supported by the India Semiconductor Mission and targets production by 2026. PSMC will provide technological support, licensing, and training. The fab will manufacture 50,000 wafers per month for applications such as power management ICs, MCUs, and logic for AI, automotive, and wireless markets.

On the other hand, a major front-end project has been put on hold which is the Adani Group – Tower Semiconductor partnership, which had proposed a € 10 billion front-end facility in Maharashtra, approved in September 2024. However, in May 2025, the Adani Group paused discussions, citing commercial uncertainty and concerns over Tower's level of financial commitment. The future of the project remains unclear.

In addition to manufacturing, India is also seeing strategic investments in design and equipment. AMD is investing € 380 million between 2023 and 2028 to expand its design capabilities, including the opening of its largest global design center in Bengaluru. Meanwhile, Lam Research has committed over € 1 billion to build a new facility in Karnataka. Signed under a memorandum of understanding with the Karnataka Industrial Area Development Board, the investment underscores confidence in India's semiconductor roadmap and will support the local production of critical semiconductor manufacturing tools.

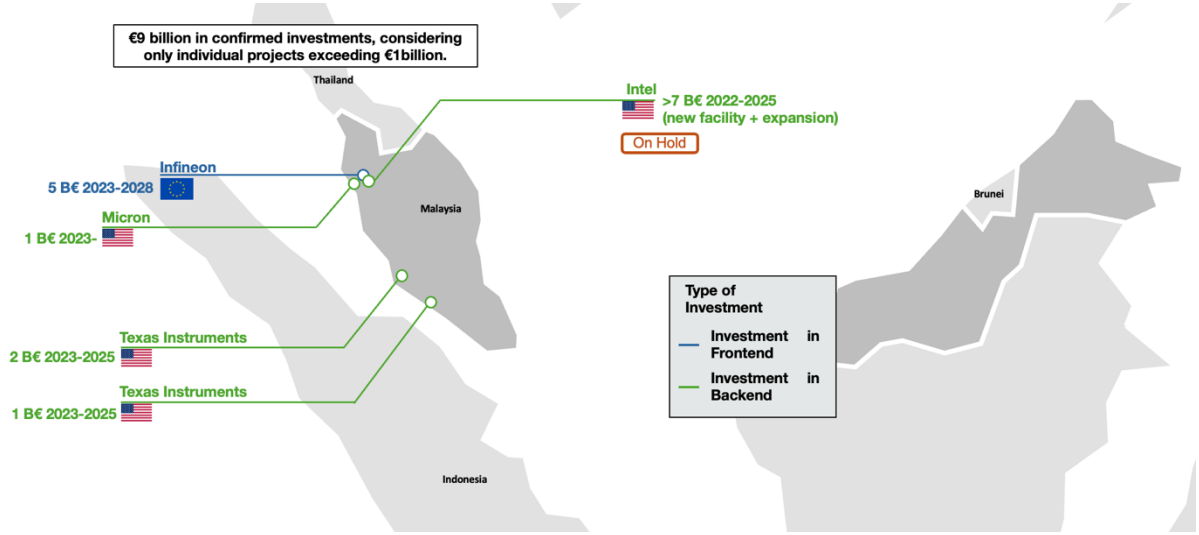
This project has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.

3.8.Malaysia

Confirmed ongoing semiconductor investments in Malaysia amount to € 9 billion, considering only individual projects exceeding € 1 billion. This represents a level of investment 5 times lower than that of the EU over the same period, and roughly equivalent to semiconductor investments in Italy.

Malaysia is a major global hub for semiconductor assembly and testing, and it is actively working to expand its role across the semiconductor value chain -particularly in advanced packaging and integrated circuit design.

Figure 25: Ongoing major investments in Malaysia, May 2025



Source: DECISION Etudes & Conseil

Texas Instruments' assembly and test factories in Kuala Lumpur and Melaka are expected to begin production late 2025. These investments, totaling over € 3 billion, reinforce the company's goal of internalizing 90% of its manufacturing by the end of the decade.

Infineon has officially opened the first phase of its Kulim 3 fab, which will become the world's largest 200-millimeter SiC power semiconductor facility. The first phase, with an investment of € 2 billion, focuses on producing silicon carbide and gallium nitride semiconductors. The second phase, estimated at up to € 5 billion, will further expand capacity and create up to 4,000 jobs. The facility will be closely integrated with Infineon's Villach site in Austria, forming "One Virtual Fab" for wide-bandgap technologies.

ASE has inaugurated its fifth plant in Penang, extending its packaging and testing capabilities. The expansion is part of a broader € 260 million plan announced in 2022 to

This project has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.

double production space. The new facility brings ASE Malaysia's total floor space to approximately 3.4 million square feet and integrates Industry 4.0 technologies and AI-driven factory automation.

In addition, Melexis has opened its largest global wafer testing facility in Kuching, Sarawak, near XFab's factory. Backed by a € 70 million investment, the new site houses 90 wafer test tools.

However, not all projects are progressing as planned. Rumors have emerged that Intel's landmark investment in Penang -once projected to be its first overseas advanced 3D packaging and wafer fabrication facility- has been put on indefinite hold. Although Intel has not confirmed this publicly, local sources report the relocation of engineers to the United States and a suspension of activity at the site.

Beyond individual projects, Malaysia is actively advancing its semiconductor strategy through national initiatives and global partnerships. A notable example is the € 215 million agreement with ARM, under which the Malaysian government will pay to access high-end chip design blueprints and technology. The deal includes training for 10,000 engineers and aims to enable local manufacturers to design and produce AI chips domestically. This initiative aligns with the objectives of the National Semiconductor Strategy (NSS), launched in 2024, which seeks to elevate Malaysia's position in the semiconductor value chain, particularly in upstream activities like chip design.

Additional efforts such as the Penang STEM Talent Blueprint and expanded TVET programs aim to develop 60,000 skilled engineers by 2030.

The government continues to offer tax incentives such as Pioneer Status (70% income tax exemption for up to 10 years) and the Investment Tax Allowance (60% allowance on capital expenditures) to attract semiconductor firms. Strategic projects such as the Wafer Fabrication Park, Advanced Packaging Program, and MYChipStart initiative further support Malaysia's vision to move up the semiconductor value chain.

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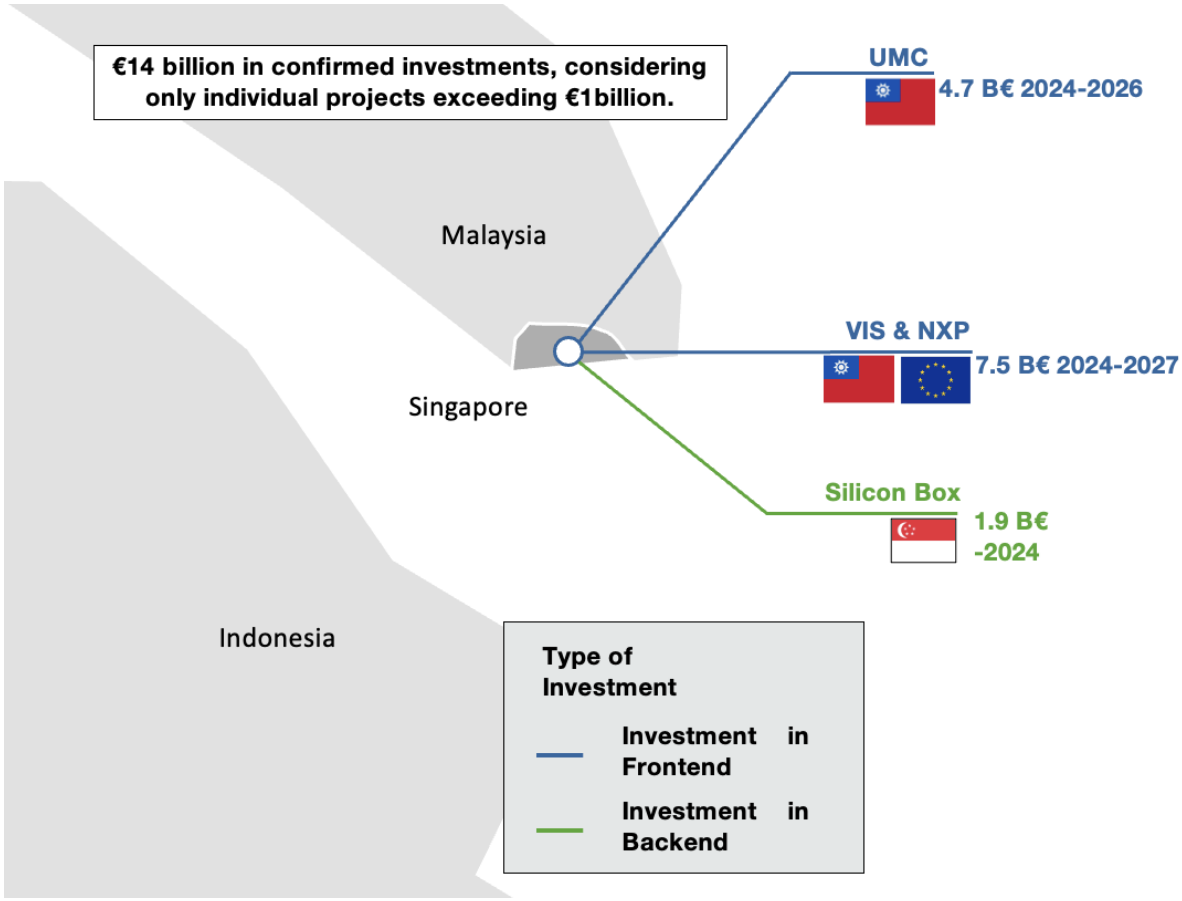
3.9.Singapore

Singapore expands its position as a strategic hub for mature-node semiconductor manufacturing, automotive chips, and advanced packaging, with € 14 billion in confirmed investments since 2023, considering only individual projects exceeding € 1 billion.

Figure 26: Ongoing investments in Singapore, May 2025



Source: DECISION Etudes & Conseil

In April 2025, UMC officially opened its new 22/28 nm fabrication facility in Pasir Ris, with volume production expected to begin in 2026. The facility represents a capital expenditure of € 4.6 billion and is expected to add 30,000 wafers per month while creating approximately 700 jobs.

In parallel, Vanguard International Semiconductor, in partnership with NXP, began construction of a new 12-inch wafer fab in mid-2024. This project, valued at € 7.2 billion, targets mass production by 2027 and focuses on analog and automotive chip production, amid growing demand for geopolitical diversification.

This project has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.

In 2024, local champion Silicon Box -specialized in chiplet packaging- invested € 1.9 billion in its first fabrication facility and in the commercialization of advanced chiplet integration technologies.

Complementing these developments, Singapore's 2025 national budget earmarked € 346 million to establish a publicly funded R&D fab under the National Semiconductor Translation and Innovation Centre (NSTIC). Scheduled to be operational by 2027, this initiative is aimed at strengthening the domestic ecosystem for prototyping, advanced packaging, and support to local startups.

This project has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.

4. The Semiconductor Talent Gap in the EU in 2025 and its Implications for Cooperation

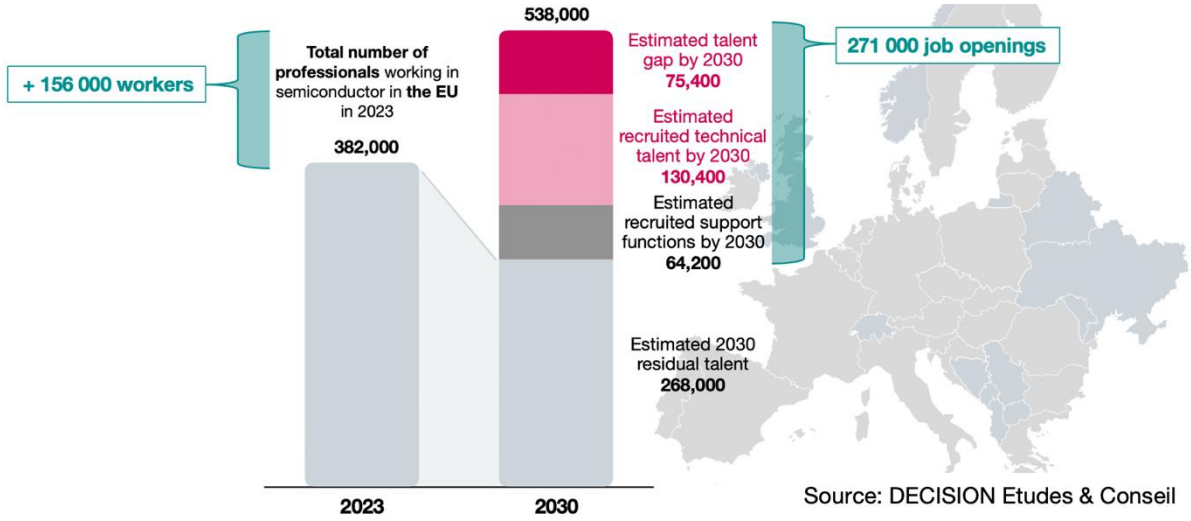
The European Skills Strategy report was published in October 2024 in the frame of the European Chips Skills Academy (ECSA) project. Prepared by DECISION Études & Conseil, the report presented the projected talent gap in the semiconductor sector across the EU27 for the 2024–2030 period, based in particular on forecasted investment plans within the EU- as illustrated in Figure 27.

According to the report, the aging of the European workforce, combined with industry growth, is expected to drive strong demand for talent: 271,000 job openings and a 5% annual increase in talent demand by 2030.

Meanwhile, the supply of graduates is expected to follow past trends, with only a 1% annual increase in semiconductor-related fields such as electronic, mechanical, software, and chemical engineering.

This imbalance between supply and demand were projected to result in a talent gap of 75,400 by 2030 -an average annual shortfall of 12,600 skilled workers, as illustrated in the map below.

Figure 27: EU Semiconductor Value Chain: Talent Gap Forecast (2024–2030)



Source: DECISION Etudes & Conseil, European Skills Strategy, ECSA, October 2024

These projections were made in mid-2024. Since then, two significant developments have affected these figures:

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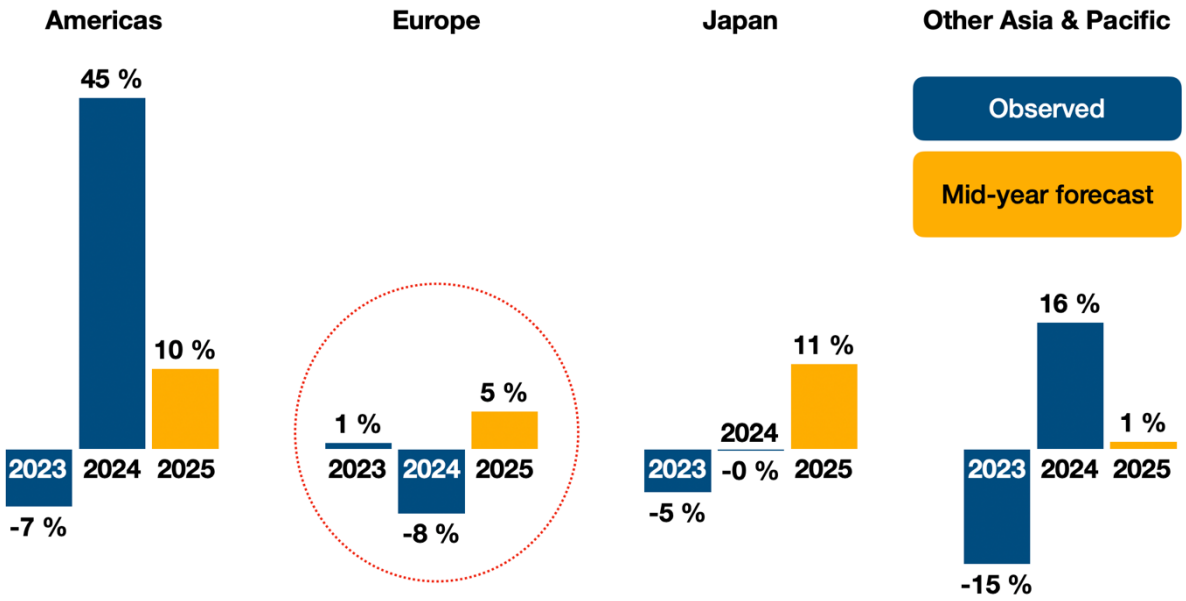
- The postponement or cancellation of four key investment projects in the EU, namely: (1) Intel's factory in Magdeburg, Germany; (2) Intel's back-end facility in Poland; (3) GlobalFoundries' investment in Crolles, France; and (4) the Wolfspeed/ZF factory in Saarland, Germany.
- The downturn of the European semiconductor market in 2024 (-8%), as shown in the diagram below, which has led several European companies to put their recruitment plans on hold.

Figure 28: Estimated Semiconductor Sales Growth for 2023–2025



Source: DECISION Etudes & Conseil, data from WSTS Spring 2025

The cancellation of the four aforementioned projects is estimated to reduce the European talent gap by approximately 7,000 people:

- Intel's investments in Magdeburg and Poland represented a potential of 5,000 direct employees by 2030.
- GlobalFoundries' investment in Crolles was expected to generate around 1,000 jobs.
- The Wolfspeed/ZF factory in Saarland was projected to create at least 600 jobs.

As for the semiconductor market downturn, its main effect is expected to be a delay in the talent shortage timeline -postponing the onset of the most critical gap by at least one year.

The EU Talent Gap Remains a Critical Issue

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Taking these two factors into account, the talent gap initially estimated at 75,400 by 2030 now stands at approximately **56,000** in June 2025, which translates to an average annual shortfall of **9,300** workers.

In other words, although the talent gap has been partially reduced and its onset delayed, it remains a significant challenge for Europe -particularly as it is expected to worsen further after 2030. Given the long lead time required to expand the skilled workforce, **urgent action is needed** to bridge this gap, especially in the regions where demand is most concentrated: **Saxony, Brainport Eindhoven, Ireland, Belgium, Crolles, Catania, Northern Italy, Bavaria, Baden-Württemberg, Czech Republic**…

Talent Cooperation Opportunities

In terms of international cooperation, beyond the exchange of PhD students and researchers with third countries on topics of mutual interest, **India and Southeast Asia** are the two regions with the **greatest surplus of graduates** in semiconductor-related fields.

Within the EU27, **Spain, Romania, Greece, Bulgaria, and Croatia** have the **largest surplus of electrical engineering graduates** relative to the current size of their national semiconductor ecosystems.

Finally, in the EU's immediate neighborhood, **Turkey and Morocco** also show a **significant surplus of electrical engineering graduates** compared to the scale of their semiconductor sectors.

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5. Results from the 2025 Survey of the EU ecosystem

5.1.Purpose

The objectives of the survey were to:

- Gather new information on the evolution of the international environment of the semiconductor industry between 2023 and 2025.
- Identify the most urgent challenges where cooperation with other countries should be initiated to the benefit of Europe.
- Obtain a prioritized list of technologies that should be supported or established as key competences in the European Union.

The survey was aimed at individuals representing or working in companies, research institutions, academia, clusters, international platforms, industry alliances, both suppliers and users of semiconductor solutions, independent technology experts and consultants.

The detailed data collected from this survey were processed by the ICOS consortium only. Statistical summaries of the data were used in the project report. By completing and submitting the survey, the respondents agreed to these terms and conditions.

The time to complete the survey was estimated for around 10min.

5.2. Survey structure

Part 1: International Cooperation Today

- Institution and Role: basic information about the respondent's institution and role
- Awareness of New Initiatives in the EU between 2023 and 2025.
- Details of New Initiatives: More details about these initiatives.

New Cooperation with a Partner from Non-EU Countries Since 2023 (First Example)

- Partner Information: Partner name and Country
- Cooperation Modality: Cooperation modality experienced
  Options: Joint co-investment in infrastructure, Joint research, Business contract, Staff exchange programme, Joint event, Other)
- Details of Cooperation: More details.

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Joint Co-Investment in Infrastructure

- Location of Joint Co-Investment: Location of the joint co-investment.
- Value of Joint Co-Investment: Value (EUR)
  Options: 0 - 1,000,000, 1,000,000 - 5,000,000, 5,000,000 - 10,000,000, 10,000,000+, I'd rather not divulge)
- Additional Details: Please provide more details.

Joint Research (First Example)

- Details of Joint Research: More details.
- Joint Budget: Joint budget (EUR)
  Options: 0 - 1,000,000, 1,000,000 - 5,000,000, 5,000,000 - 10,000,000, 10,000,000+, I'd rather not divulge

Business Contract

- Role of Non-EU Partner: What was the role of your non-EU partner?
  Options: Supplier, Client
- Value of Business Contract: Value (EUR)
  Options: 0 - 1,000,000, 1,000,000 - 5,000,000, 5,000,000 - 10,000,000, 10,000,000+, I'd rather not divulge
- Additional Details: Please provide more details.

Staff Exchange Programme

- Participants in Exchange Programme: Which staff took part in the exchange programme?
  Options: Management, Research staff, Students, PhD students, Back-office staff
- Number of Participants: Number of participants in the entire exchange programme.
- Additional Details: Please provide more details.

Joint Event

- Type of Event: What type of event did you collaborate on?
  Options: Conference, Fair, Study visit, Workshop, Other

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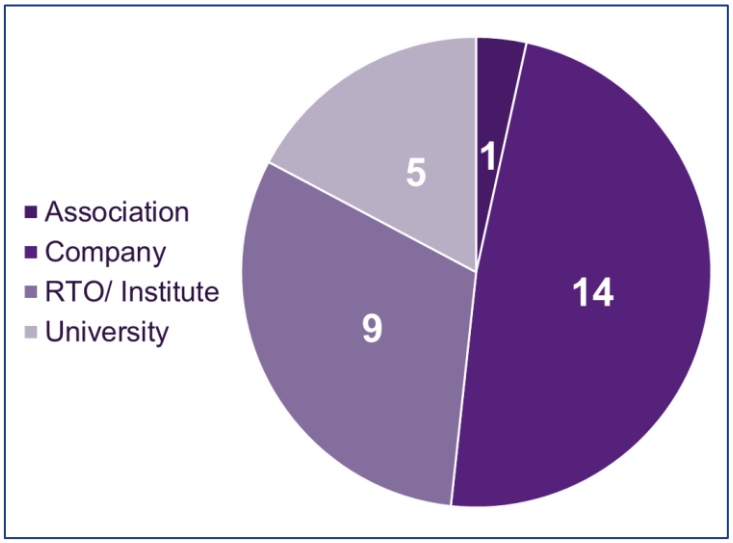
- Mode of Participation: What was the mode of participation in the event? Options: On-site, Online, Hybrid
- Number of Participants: How many people participated in the event?
- Additional Details: Please provide more details.

5.3. Survey results

As a result of the engagement campaign launched through the ICOS social media accounts and individual invitation shared by the project partners in total 32 answers gathered.

Most answers came from companies 14, followed by 9 answers from representatives of RTOs or Institutes – 9 than Universities – 5 and one association – 1.

Figure 29. Survey respondents' affiliation



Source: Own elaboration, survey results.

When considering the role of the respondents in their organisation managers counted for 20, researchers – 8 and specialists – 3.

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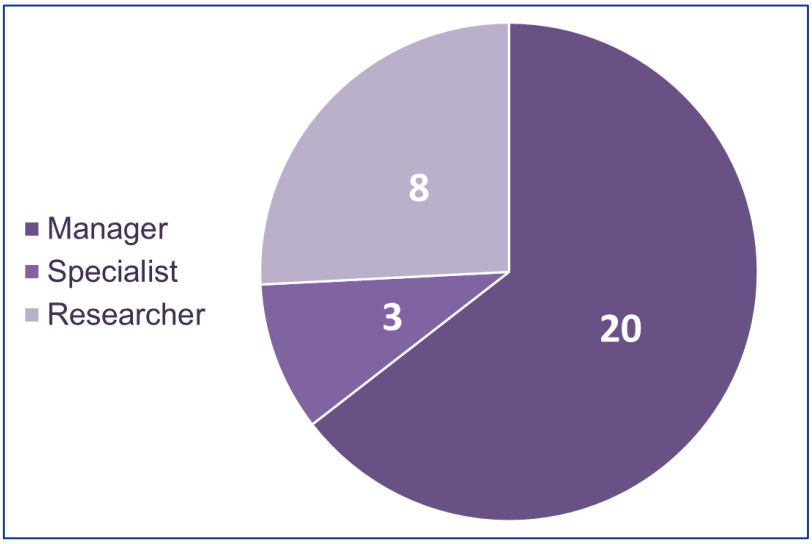
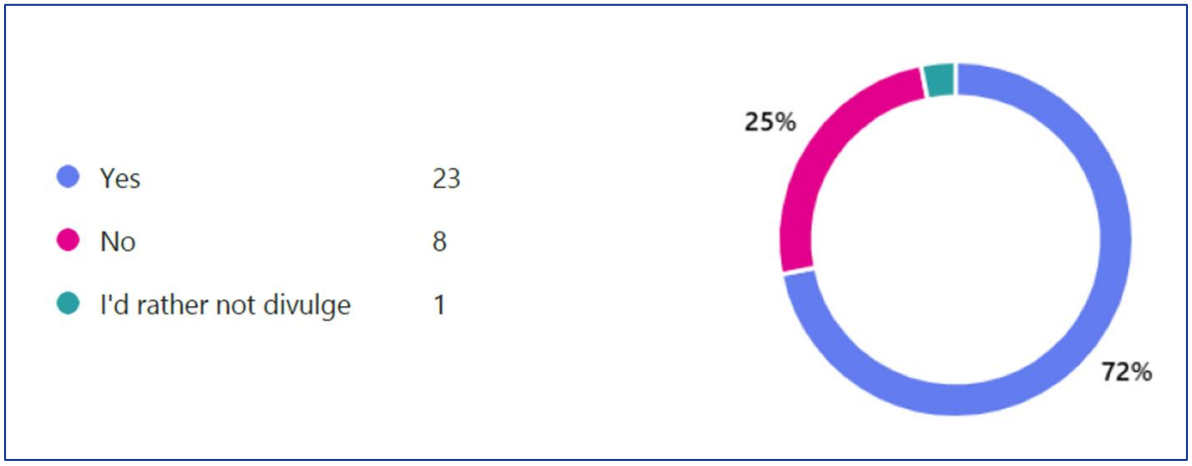
Figure 30. Survey respondents' function.



Source: Own elaboration, survey results.

23 respondents clearly confirmed some new initiatives or investments in semiconductors in the European Union between 2023 and 2025, 8 not and 1 person likely knew about something but did not want to divulge any details.

Figure 31. Survey respondents' function.



Source: Own elaboration, survey results.

In terms of subject the answers can be group as following:

Chips JU and Related Initiatives

- Pilot Lines in Chips JU (FAMES, APECS, Quantum PLs), Chips Competence Centres (POEMS), EURO-CDP (DECIDE) Design Platform,

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- IPCEI ME/CT / Eureka Cluster XECS

Quantum Computing and Neuromorphic Computing

- CMOS-based scalable device and integration technologies for quantum computing
- Neuromorphic computing focusing on materials, devices, circuit design, algorithm, and applications

Regional or national semiconductor platforms or programmes

- Romanian National Semiconductors Platform,
- FMD-QNC, Bayerisches Chip-Design-Center (BCDC)
- National Growthfund within the Netherlands, focusing on integrated photonics, heterogeneous integration, and quantum computing

AI and Advanced Technologies

- Increased use of AI & LLM leading to higher power consumption and solutions to cope with it
- Investigations towards chiplets and use of AI for design

Companies

- ESMC in Germany
- AMS OSRAM production expansion
- ST Microelectronics chips plant in Italy
- HyperPIC project funded through IPCEI ME/CT for VIGO Photonics, Poland

Since 2023, a new cooperation in the field of semiconductors with a partner from a non-EU country:

Total Instances of Cooperation

- 22 instances of cooperation with non-EU partners.

Partner Countries Involved

- USA: 7

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- South Korea: 5
- Japan: 3
- Canada: 2
- Taiwan: 2
- China: 1
- Turkey: 1
- UK: 1

Types of Cooperation Modalities

- Joint research: 12
- Business contract: 5
- Joint co-investment in infrastructure: 3
- Staff exchange program: 2

Cooperation Details

- Funding Value:
  - 1,000,000 - 5,000,000 EUR: 5
  - 0 - 1,000,000 EUR: 2
  - 5,000,000 - 10,000,000 EUR: 2
  - Confidential: 2

Details on cooperation with non-EU individual countries

USA

- Joint research: US-Ireland scheme.
- Joint research: Development of new materials for BEOL devices.
- Joint research: Various joint research projects with Portuguese programs and universities.
- Business contract: Supplier for automotive computing.

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- Business contract: Providing design services on CMOS and GaN technologies.
- Business contract: Utilizing 3rd party OSAT for standard chip assembly and custom package development.
- Staff exchange program: Photonic integration technical business training.

South Korea

- Joint research: Hardware security, post-quantum cryptography.
- Joint research: Co-development of a thin-film phototransistor for single-molecule detection in electrolytes.
- Joint research: Memristors.
- Joint research: Various joint research projects with Portuguese programs and universities
- Staff exchange program: One PhD student to visit KTH.

Japan

- Joint co-investment in infrastructure: R&D laboratories, factory, others.
- Joint research: Development of new materials for More Moore applications.
- Joint research: Various joint research projects with Portuguese programs and universities.

Canada

- Business contract: Supplier, transfer of IP.
- Takeover: Infineon took over GaN Systems.

Taiwan

- Joint co-investment in infrastructure: R&D laboratories, factory, others.
- Joint research, staff exchange, and trainings: Common projects related to microelectronics and photonics.

China

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- Joint research: Various joint research projects with Portuguese programs and universities.

Other Associated Countries (Turkey, UK)

- Joint research: Various joint research projects with Portuguese programs and universities.

5.4. Conclusions

Importance of International Collaboration

Since 2023, there have been 22 new instances of cooperation with non-EU countries, highlighting the increasing need for global partnerships in the semiconductor sector. The most frequent partners were the USA, South Korea, and Japan, indicating Europe's strategic alignment with global technology leaders.

Joint Research as the Dominant Collaboration Mode

Joint research projects were the most common form of cooperation (12 out of 22), reflecting a strong emphasis on knowledge exchange and collaborative innovation. Other forms such as business contracts, infrastructure co-investments, and staff exchange programs were also present but less frequent.

Diverse Technological Focus Areas

The collaborations covered a wide range of topics, including quantum and neuromorphic computing, chiplet architectures, and AI-driven chip design. This diversity reflects the dynamic evolution of the semiconductor landscape and the need for specialization across multiple domains.

Positive Impact of New EU Initiatives

European initiatives such as Chips JU, IPCEI ME/CT, and national platforms in Germany, the Netherlands, and Romania are well recognized and serve as a foundation for further cooperation. These programs are seen as essential for building Europe's technological sovereignty.

Strong Involvement of the Private Sector

Most respondents came from companies (14 out of 32), with managers being the dominant professional group. This indicates that the private sector is actively engaged in shaping international strategies and partnerships in semiconductors.

This project has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.

Need for Further Support and Coordination

Despite positive examples, the overall number of collaborations remains limited. This suggests a need for better coordination, financial support, and matchmaking platforms to facilitate new partnerships and scale up existing ones.

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